US009349841B2

(12) **United States Patent**
Huang et al.

(10) **Patent No.: US 9,349,841 B2**
(45) **Date of Patent: May 24, 2016**

(54) **FINFETS AND METHODS FOR FORMING THE SAME**

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(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/625,848**

(22) Filed: **Feb. 19, 2015**

(65) **Prior Publication Data**

US 2015/0171187 A1 Jun. 18, 2015

Related U.S. Application Data

(62) Division of application No. 13/779,356, filed on Feb. 27, 2013, now Pat. No. 8,987,791.

(51) **Int. Cl.**

H01L 29/34	(2006.01)
H01L 29/66	(2006.01)
H01L 29/78	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 29/6681*** (2013.01); ***H01L 21/30604*** (2013.01); ***H01L 21/3247*** (2013.01); ***H01L 29/0653*** (2013.01); ***H01L 29/34*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/7853*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/6681; H01L 29/34; H01L 21/30604; H01L 21/3247; H01L 29/0653

See application file for complete search history.

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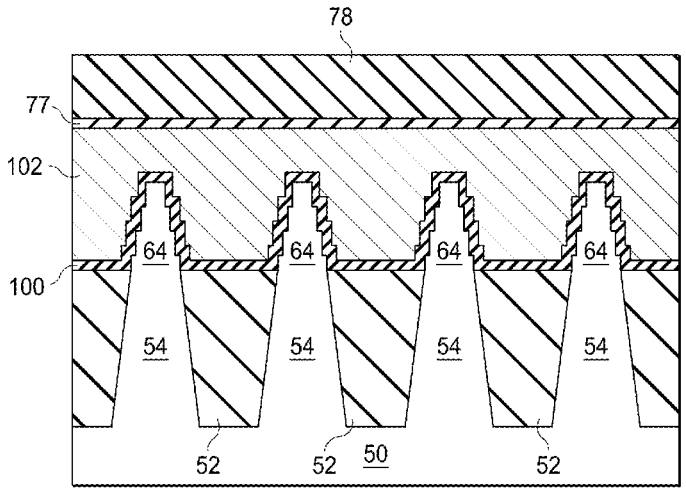
Assistant Examiner — Fazli Erdem
(74) *Attorney, Agent, or Firm* — Slater Matsil, LLP

(57) **ABSTRACT**

A finFET and methods for forming a finFET are disclosed. A structure comprises a substrate, a fin, a gate dielectric, and a gate electrode. The substrate comprises the fin. The fin has a major surface portion of a sidewall, and the major surface portion comprises at least one lattice shift. The at least one lattice shift comprises an inward or outward shift relative to a center of the fin. The gate dielectric is on the major surface portion of the sidewall. The gate electrode is on the gate dielectric.

20 Claims, 23 Drawing Sheets



(51) **Int. Cl.**

H01L 21/306	(2006.01)
H01L 21/324	(2006.01)
H01L 29/06	(2006.01)

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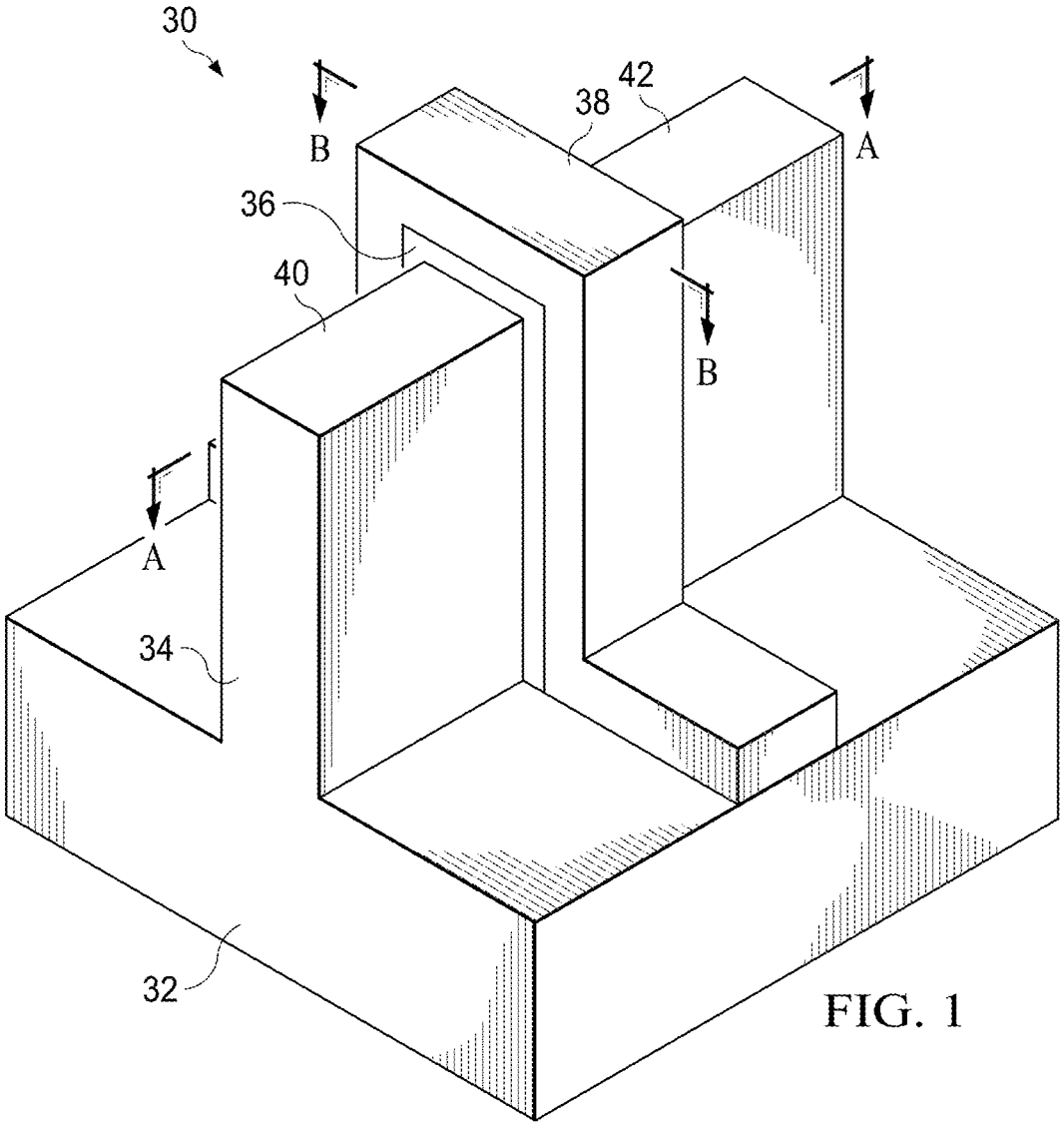


FIG. 1

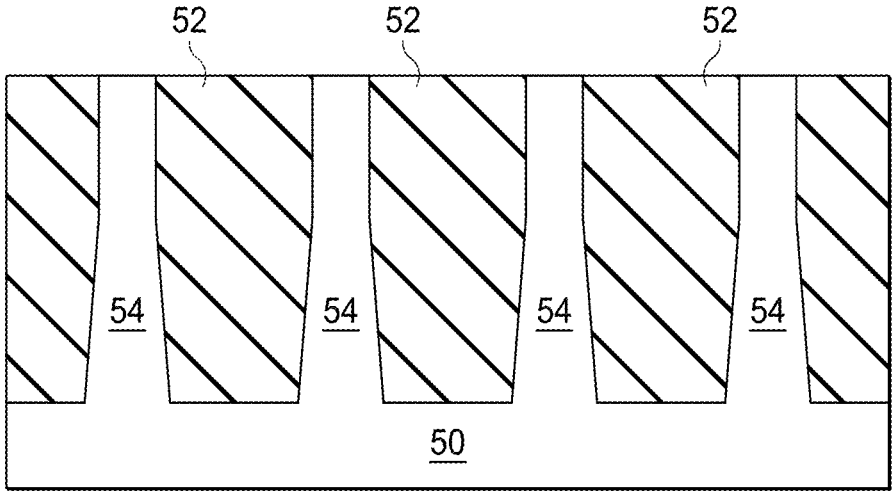


FIG. 2

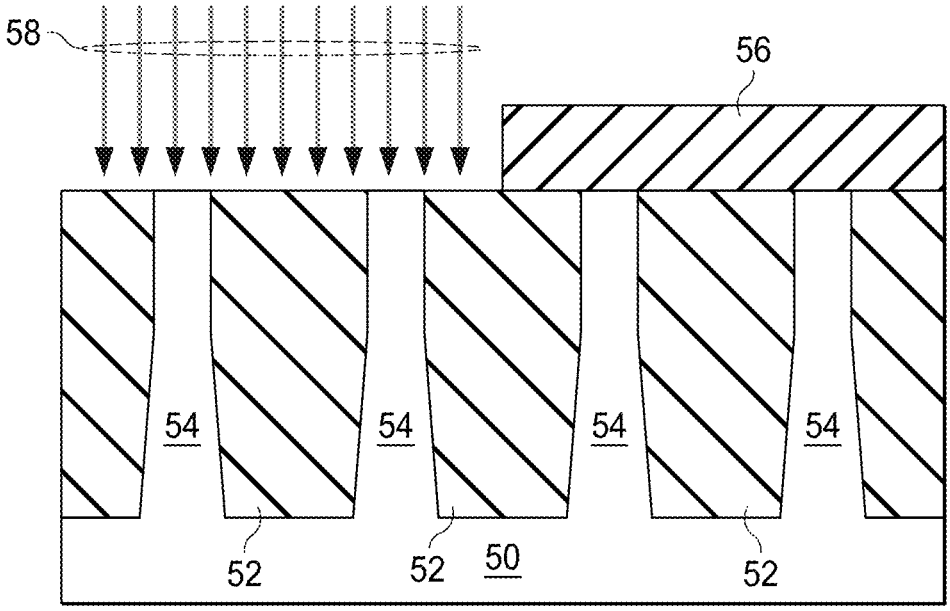


FIG. 3

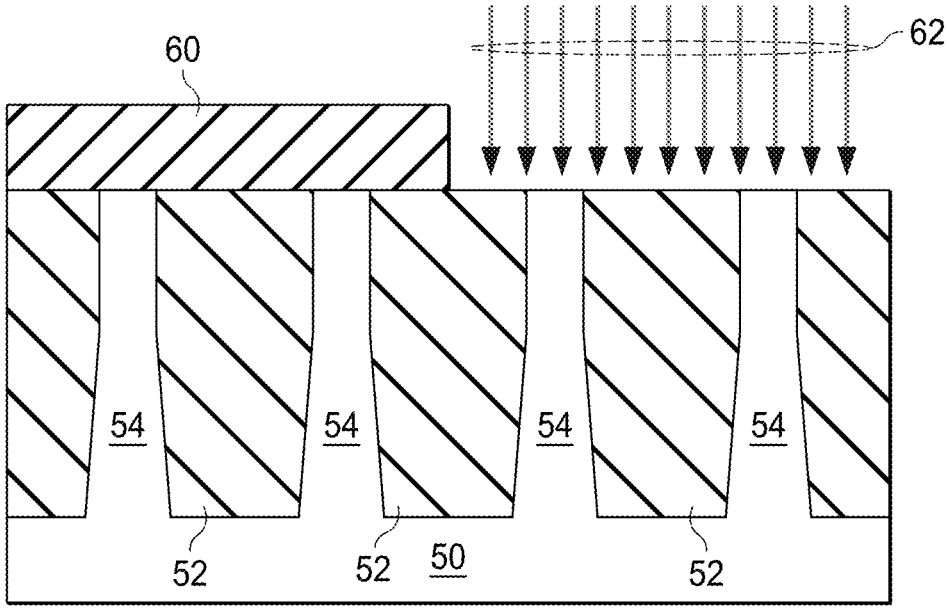


FIG. 4

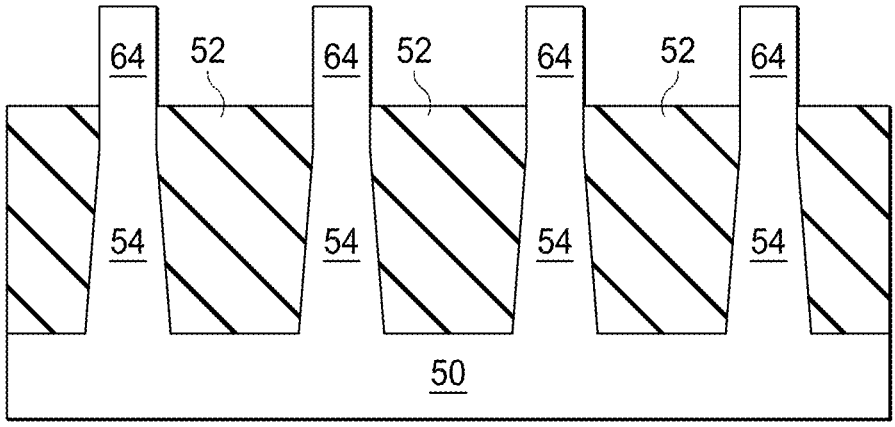
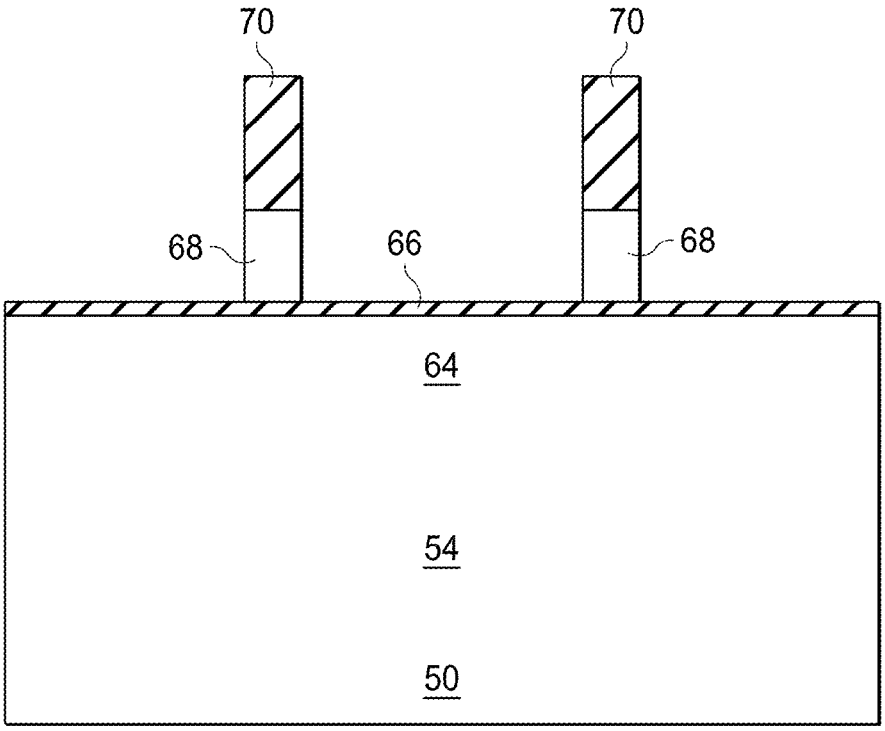


FIG. 5


70
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68
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FIG. 6A

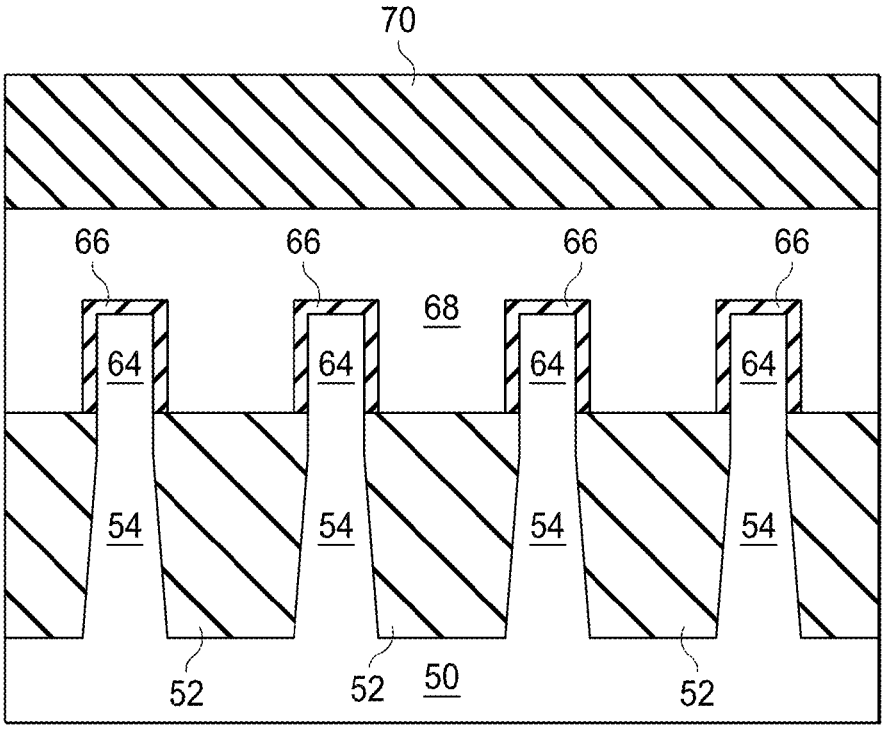
70
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FIG. 6B

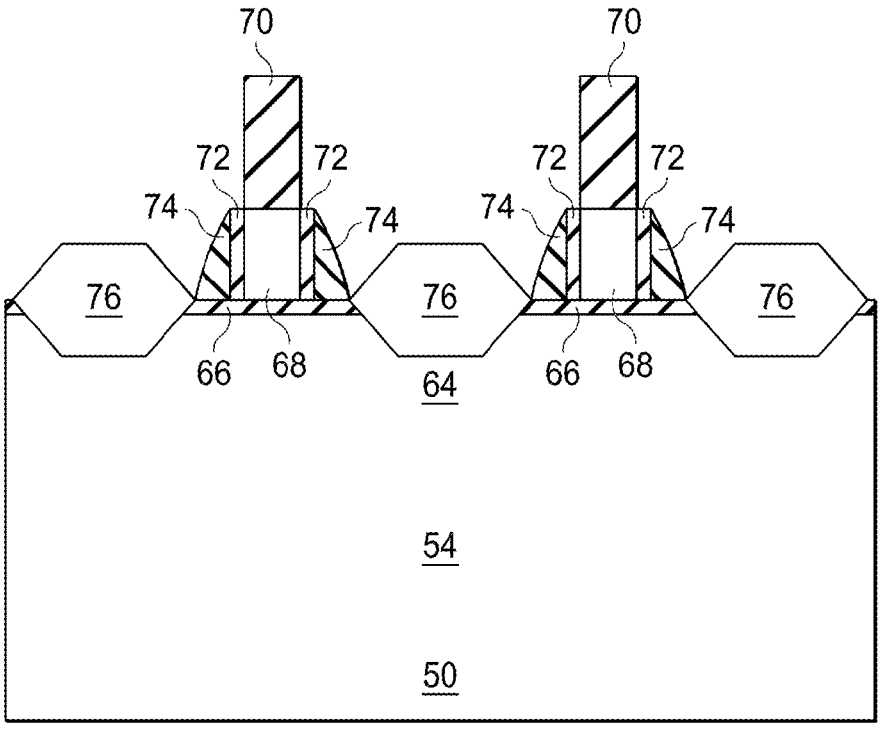
70
70
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FIG. 7A

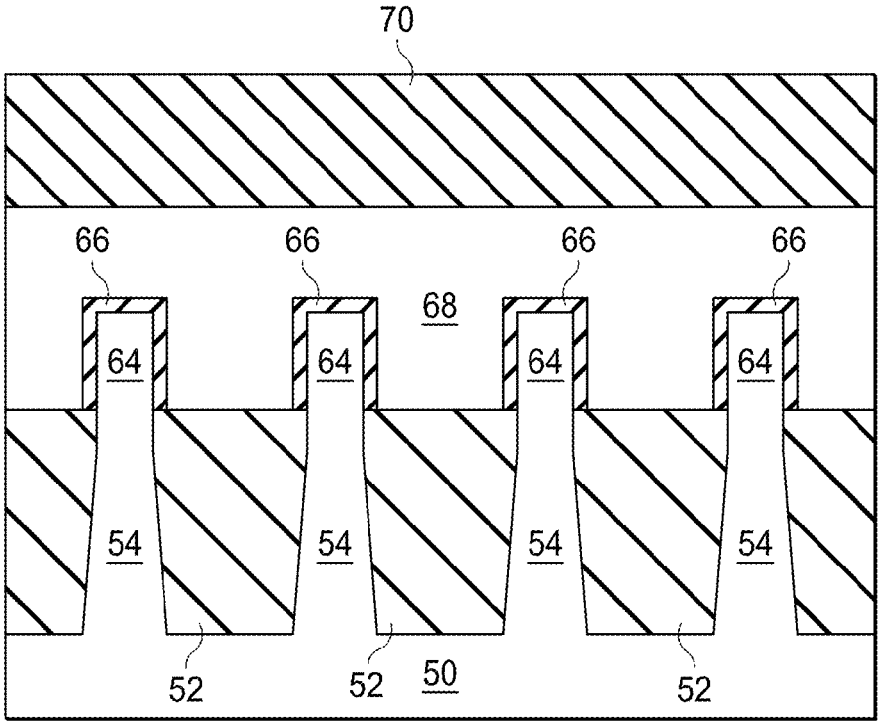
70
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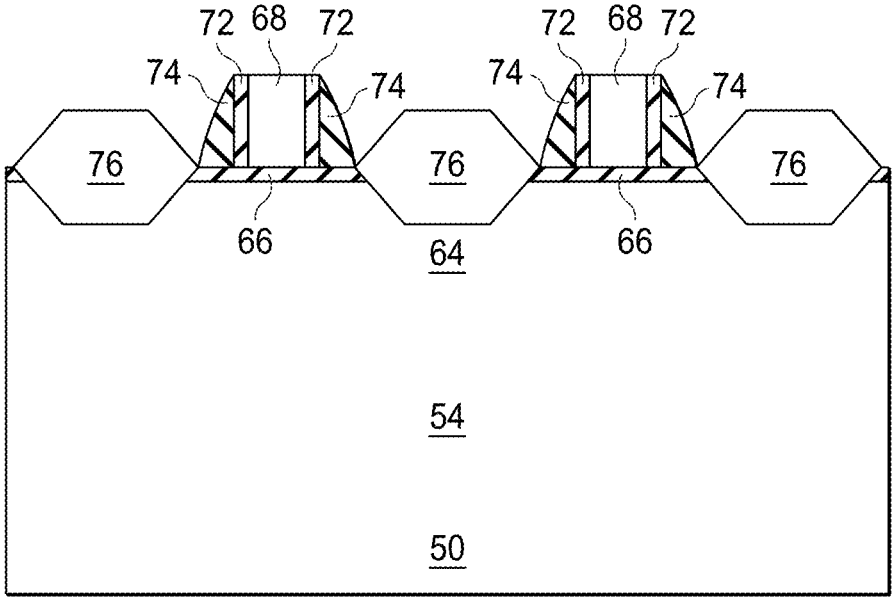
FIG. 7B


72
68
72
74
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72
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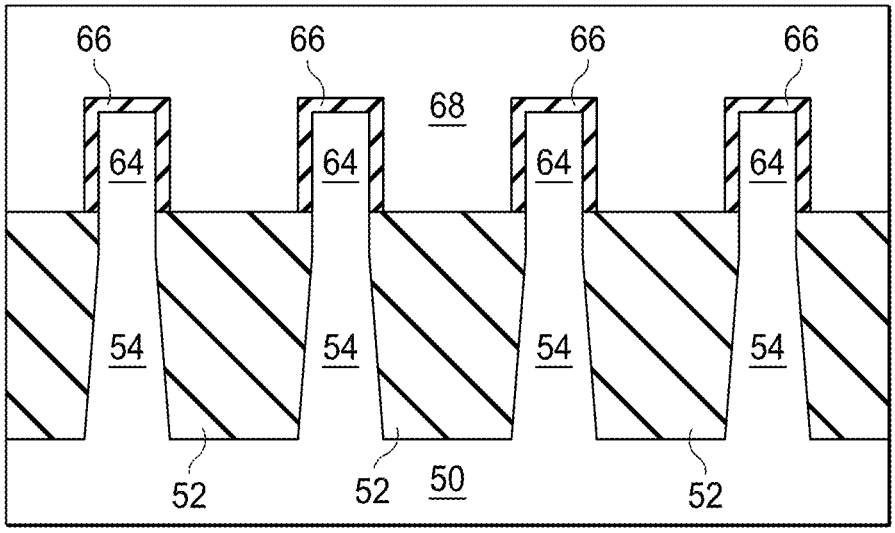
FIG. 8A


66
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66
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FIG. 8B

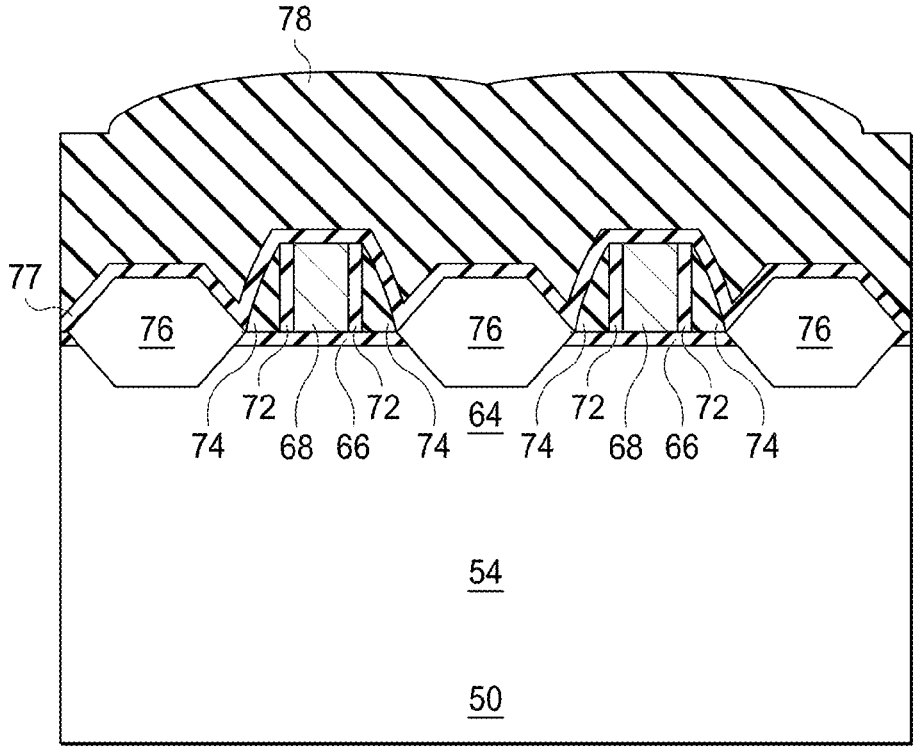
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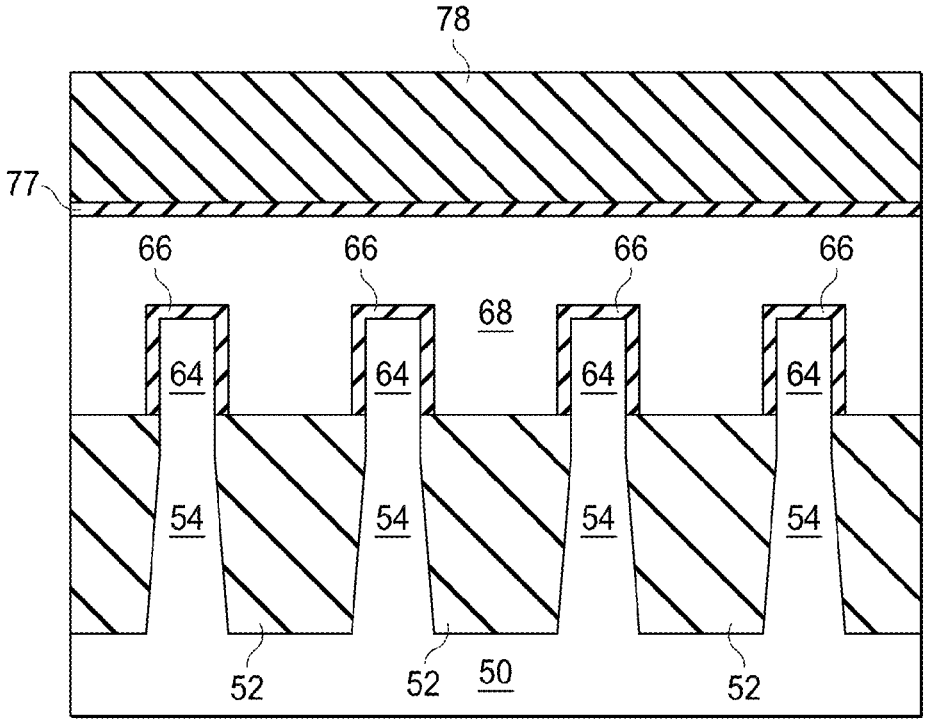
FIG. 9A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66
66
66
66
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64
64
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FIG. 9B

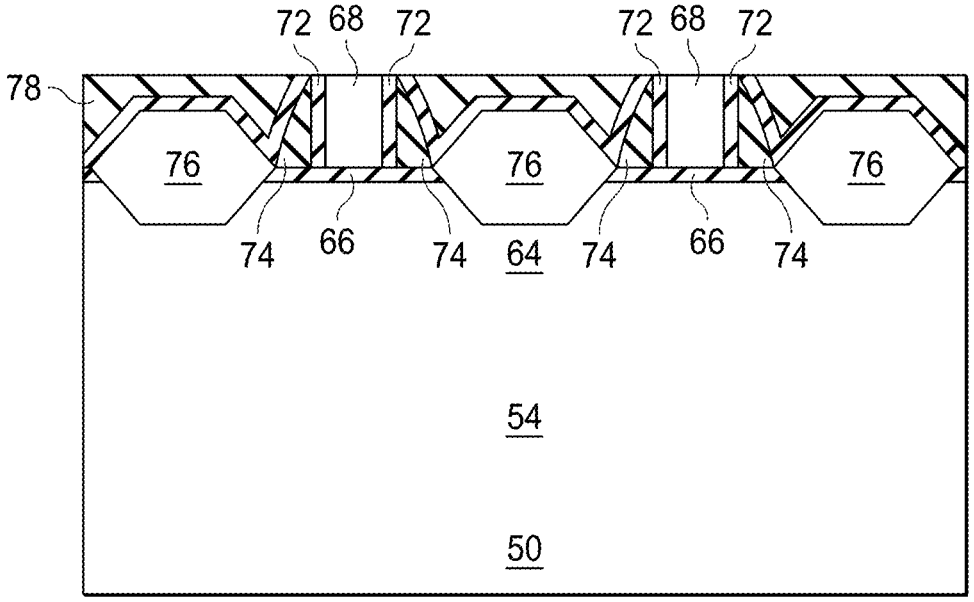


FIG. 10A

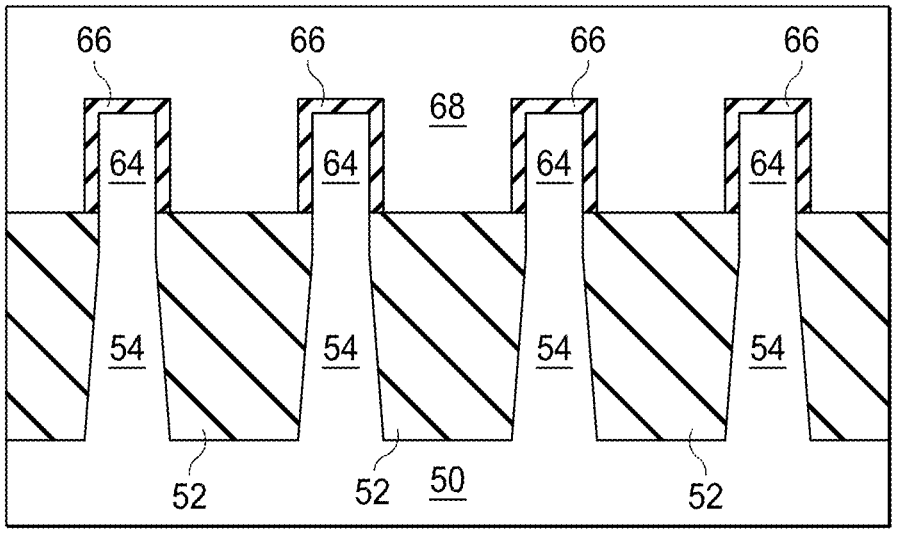


FIG. 10B

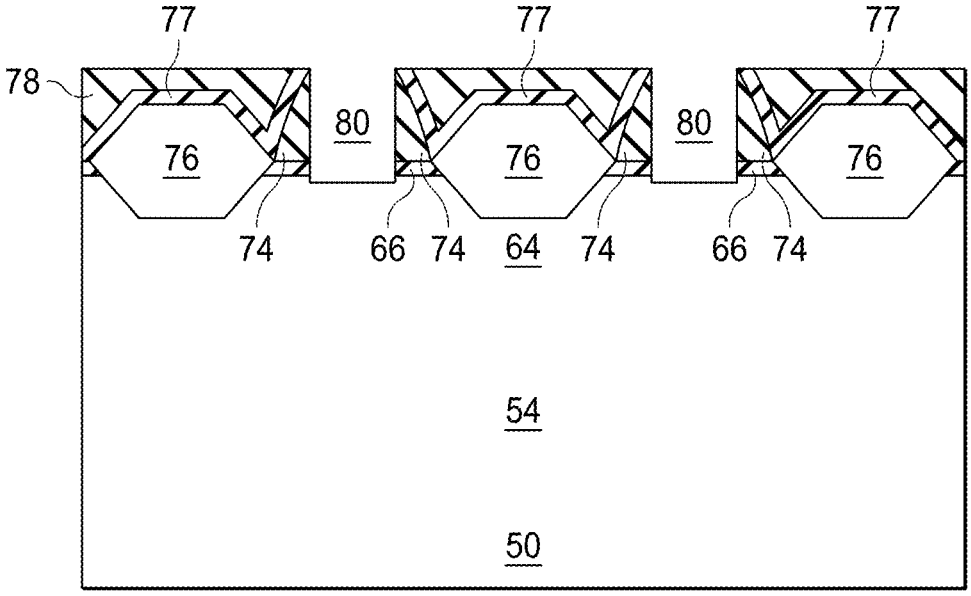


FIG. 11A

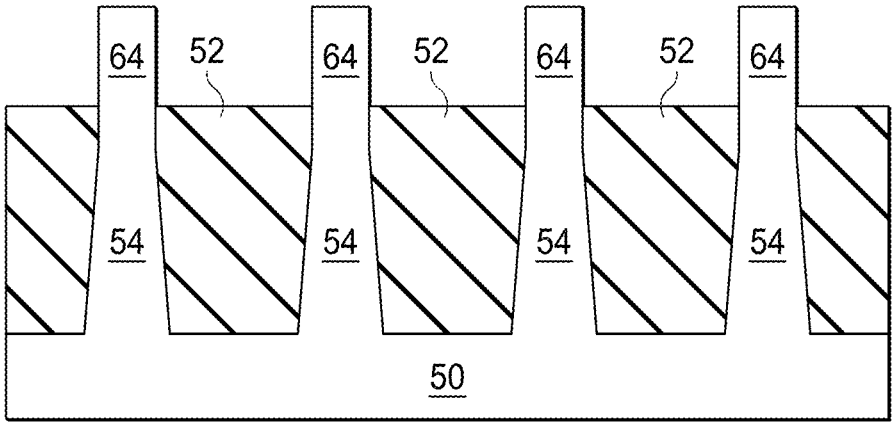


FIG. 11B

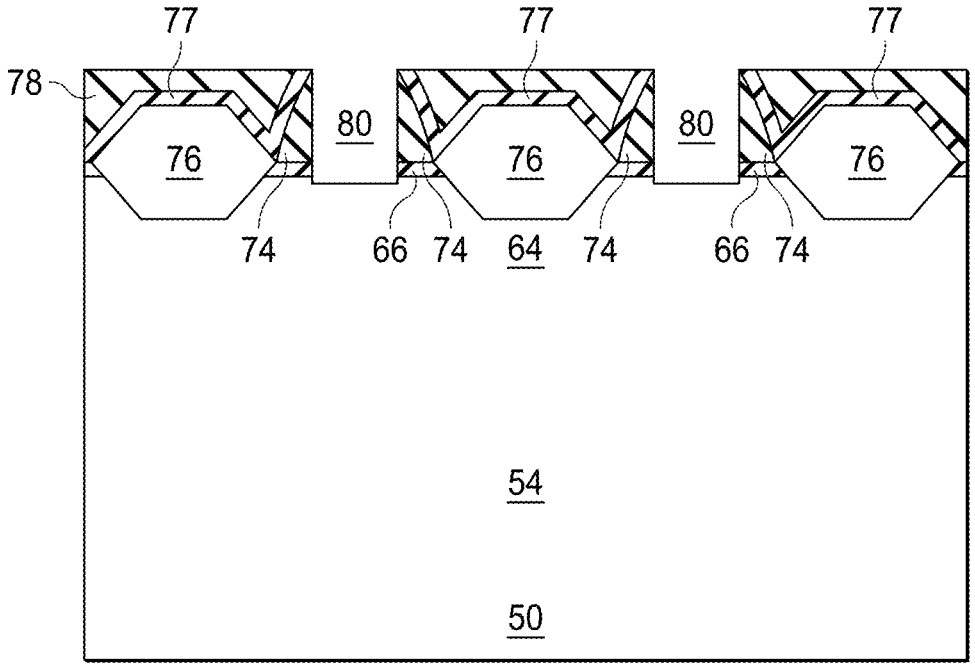


FIG. 12A

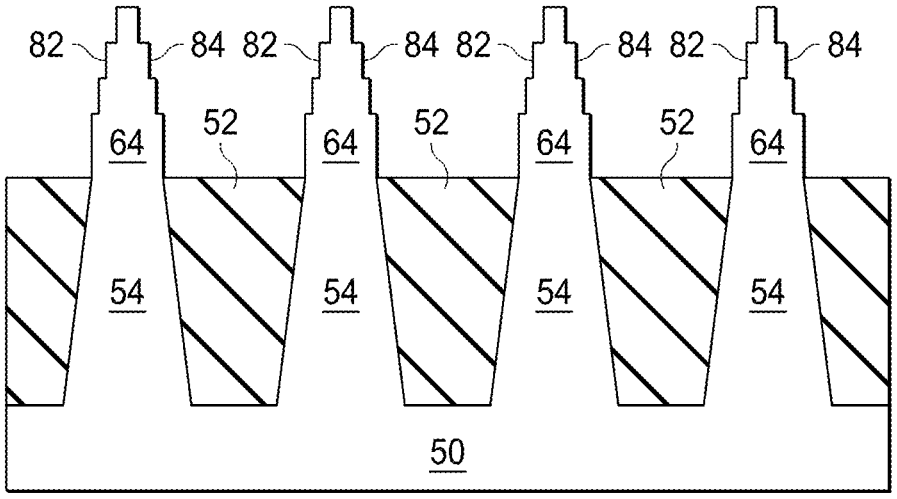


FIG. 12B

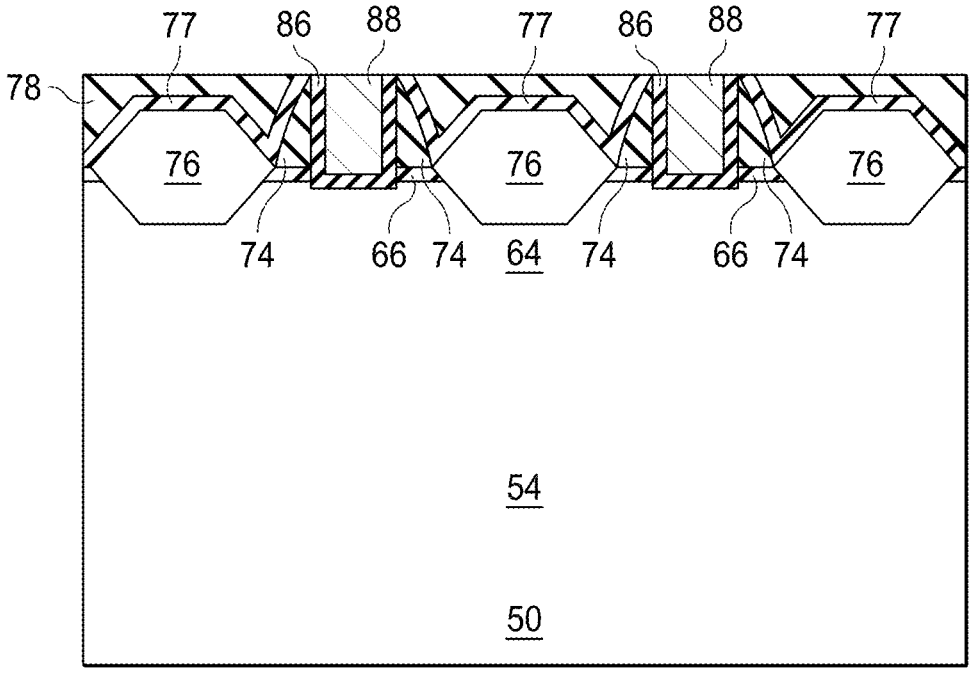


FIG. 13A

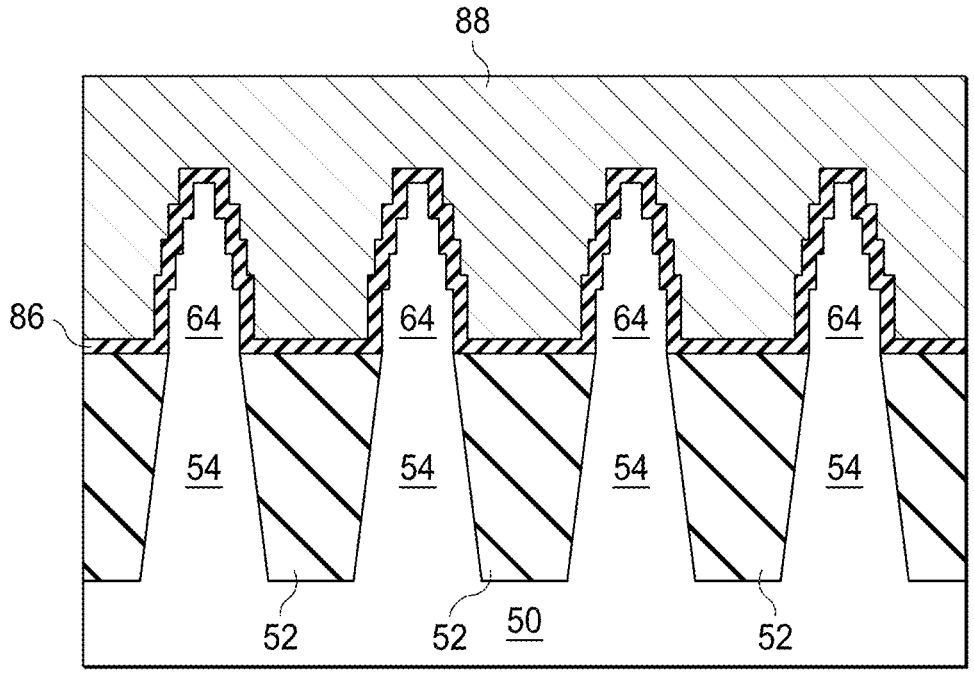


FIG. 13B

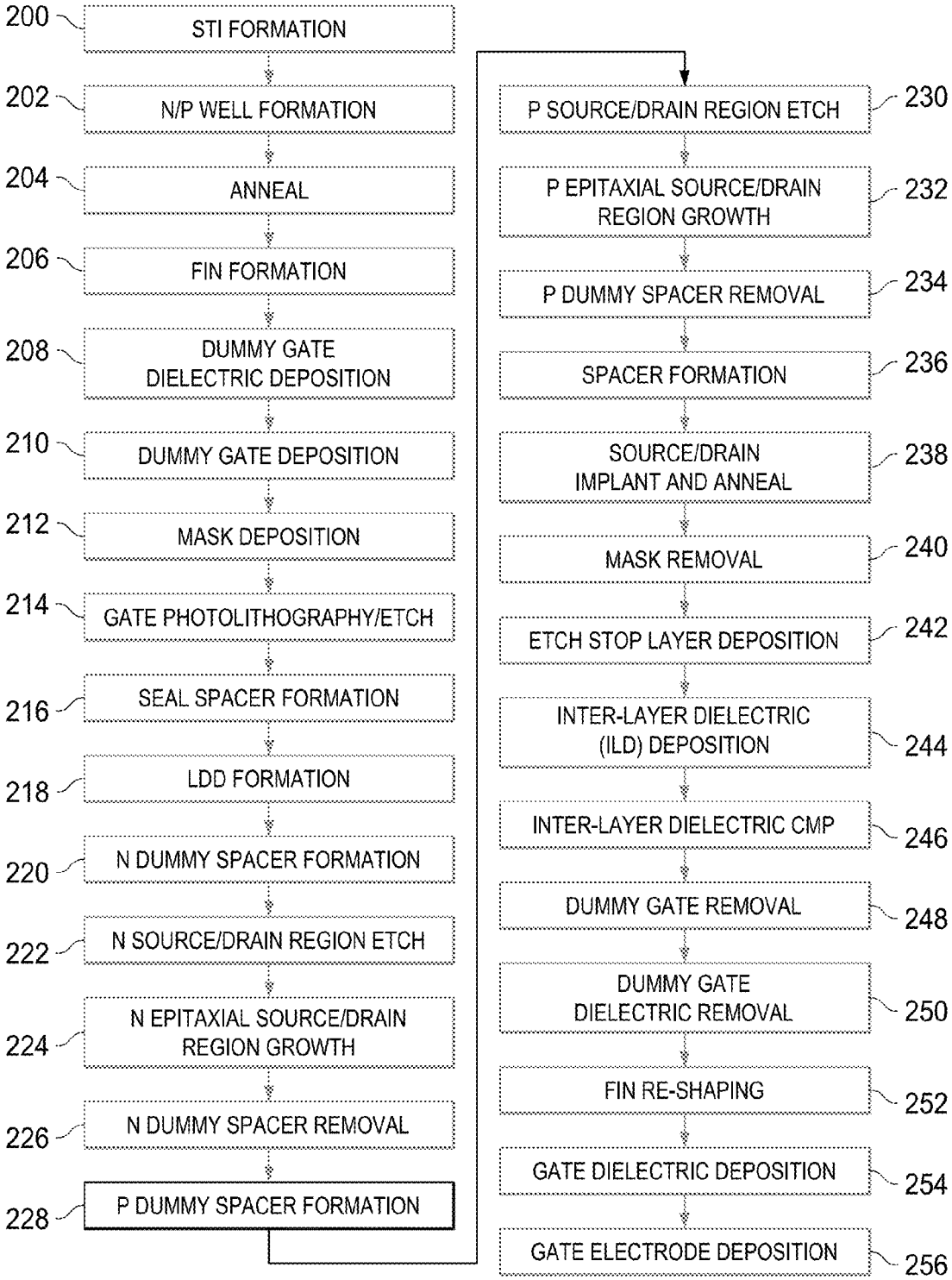

200
STI FORMATION
202
N/P WELL FORMATION
204
ANNEAL
206
FIN FORMATION
208
DUMMY GATE DIELECTRIC DEPOSITION
210
DUMMY GATE DEPOSITION
212
MASK DEPOSITION
214
GATE PHOTOLITHOGRAPHY/ETCH
216
SEAL SPACER FORMATION
218
LDD FORMATION
220
N DUMMY SPACER FORMATION
222
N SOURCE/DRAIN REGION ETCH
224
N EPITAXIAL SOURCE/DRAIN REGION GROWTH
226
N DUMMY SPACER REMOVAL
228
P DUMMY SPACER FORMATION
230
P SOURCE/DRAIN REGION ETCH
232
P EPITAXIAL SOURCE/DRAIN REGION GROWTH
234
P DUMMY SPACER REMOVAL
236
SPACER FORMATION
238
SOURCE/DRAIN IMPLANT AND ANNEAL
240
MASK REMOVAL
242
ETCH STOP LAYER DEPOSITION
244
INTER-LAYER DIELECTRIC (ILD) DEPOSITION
246
INTER-LAYER DIELECTRIC CMP
248
DUMMY GATE REMOVAL
250
DUMMY GATE DIELECTRIC REMOVAL
252
FIN RE-SHAPING
254
GATE DIELECTRIC DEPOSITION
256
GATE ELECTRODE DEPOSITION

FIG. 14

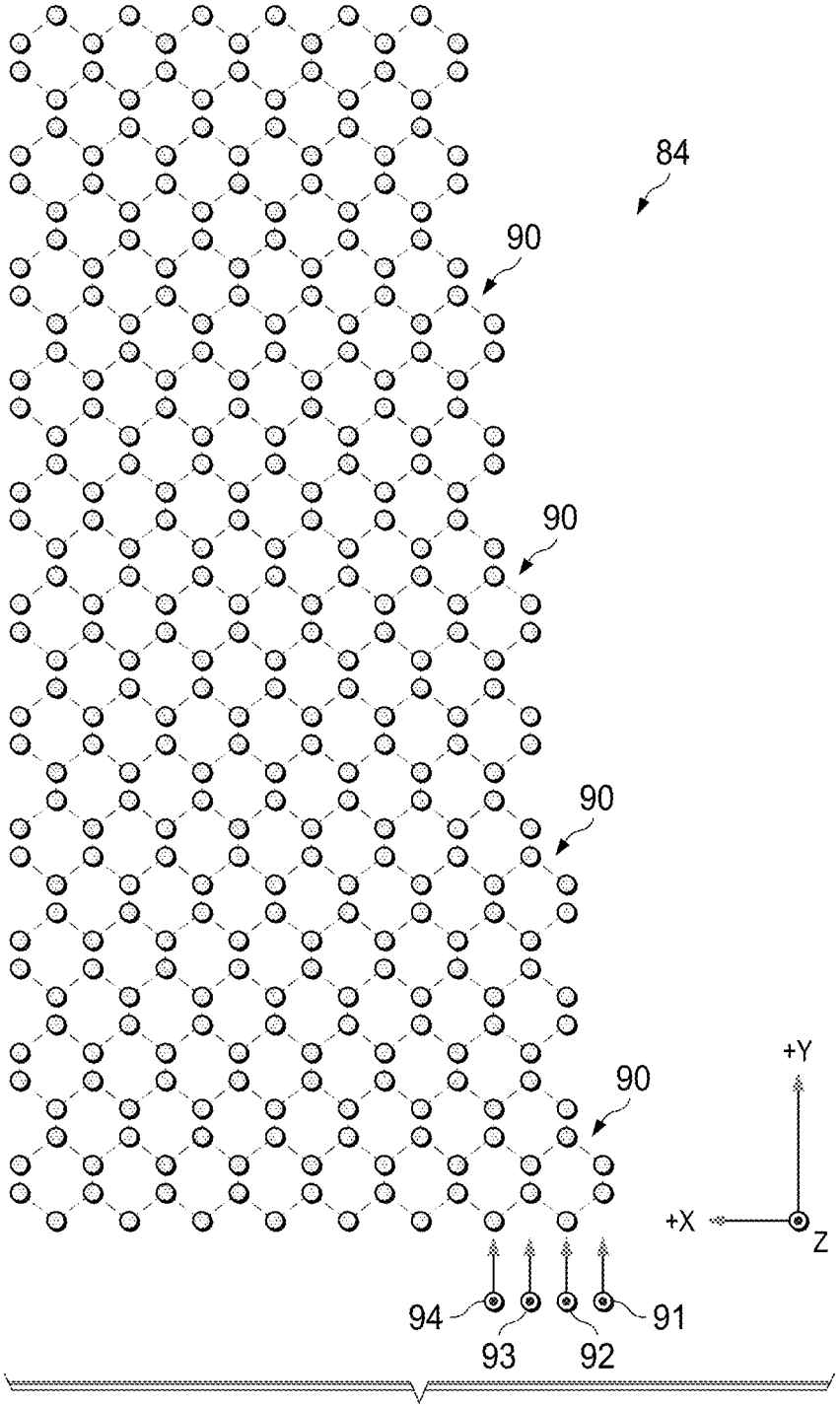


FIG. 15

FIG. 16

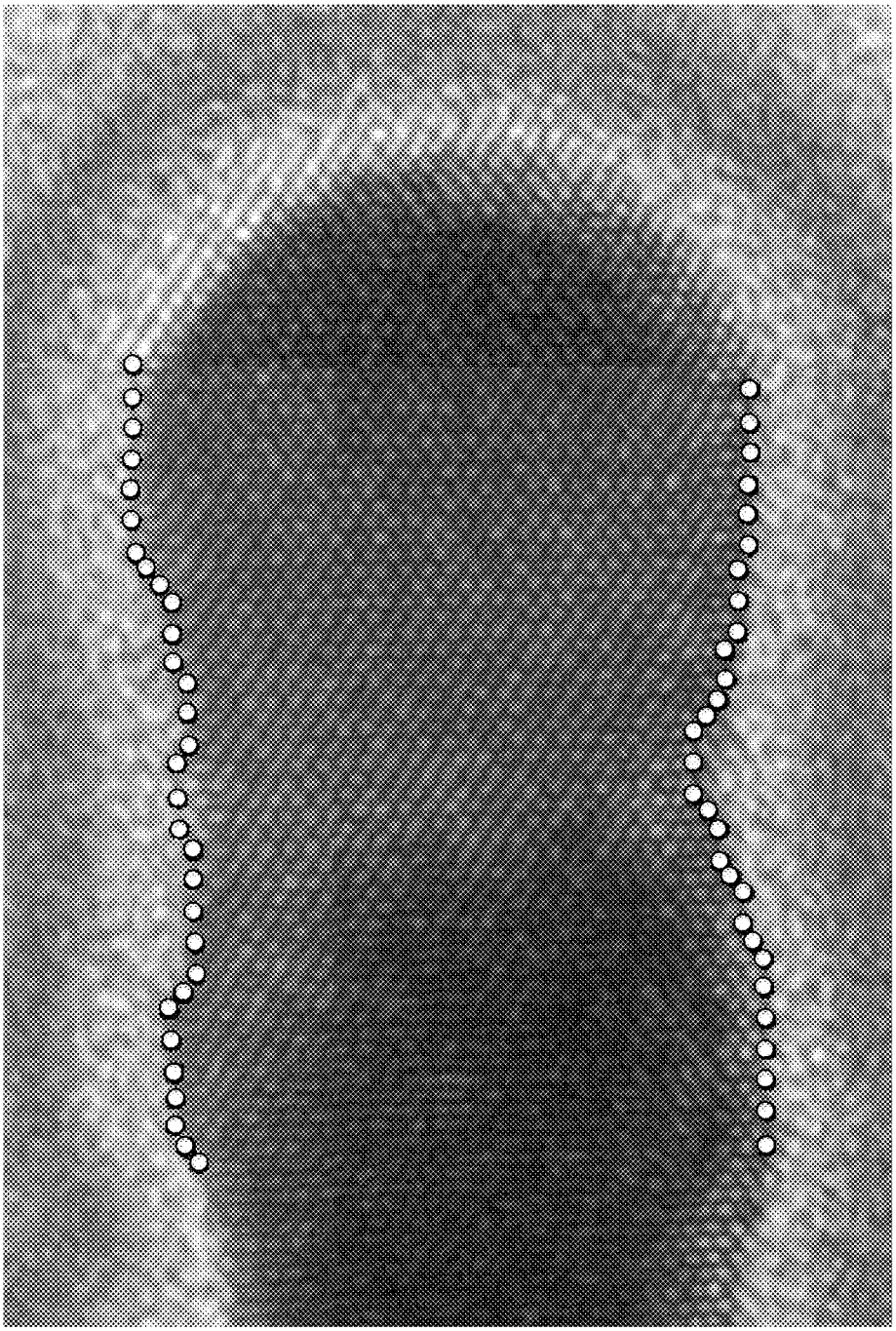


FIG. 17

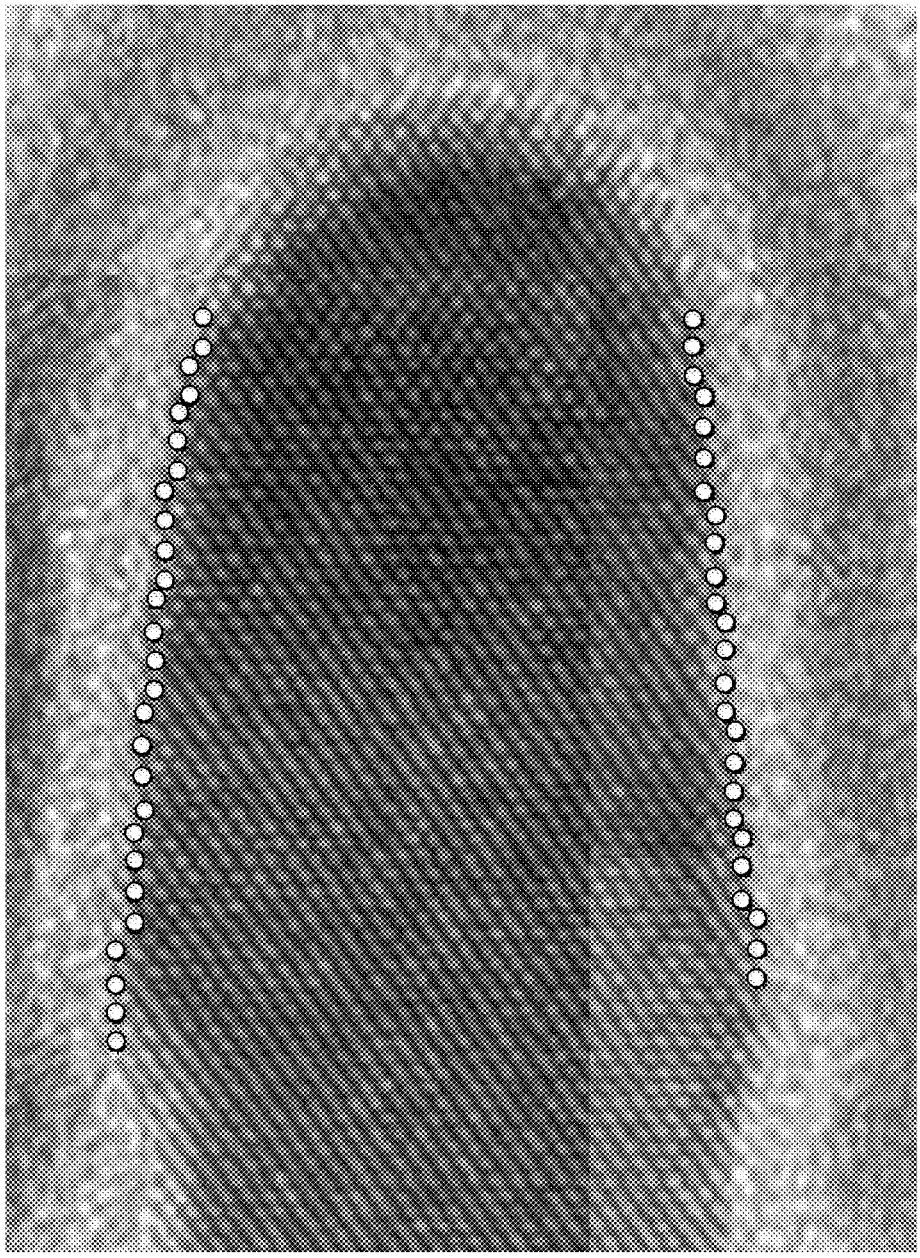


FIG. 18

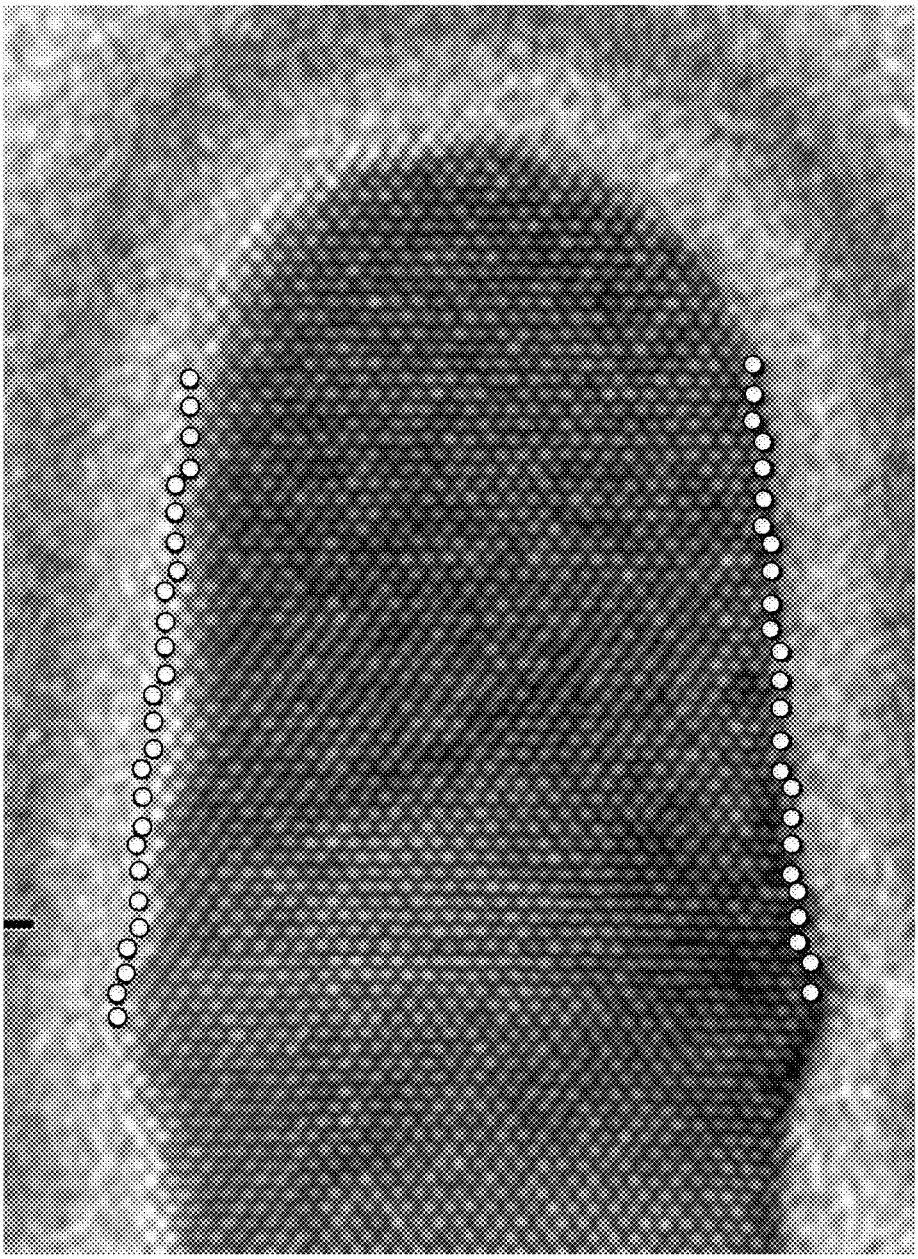
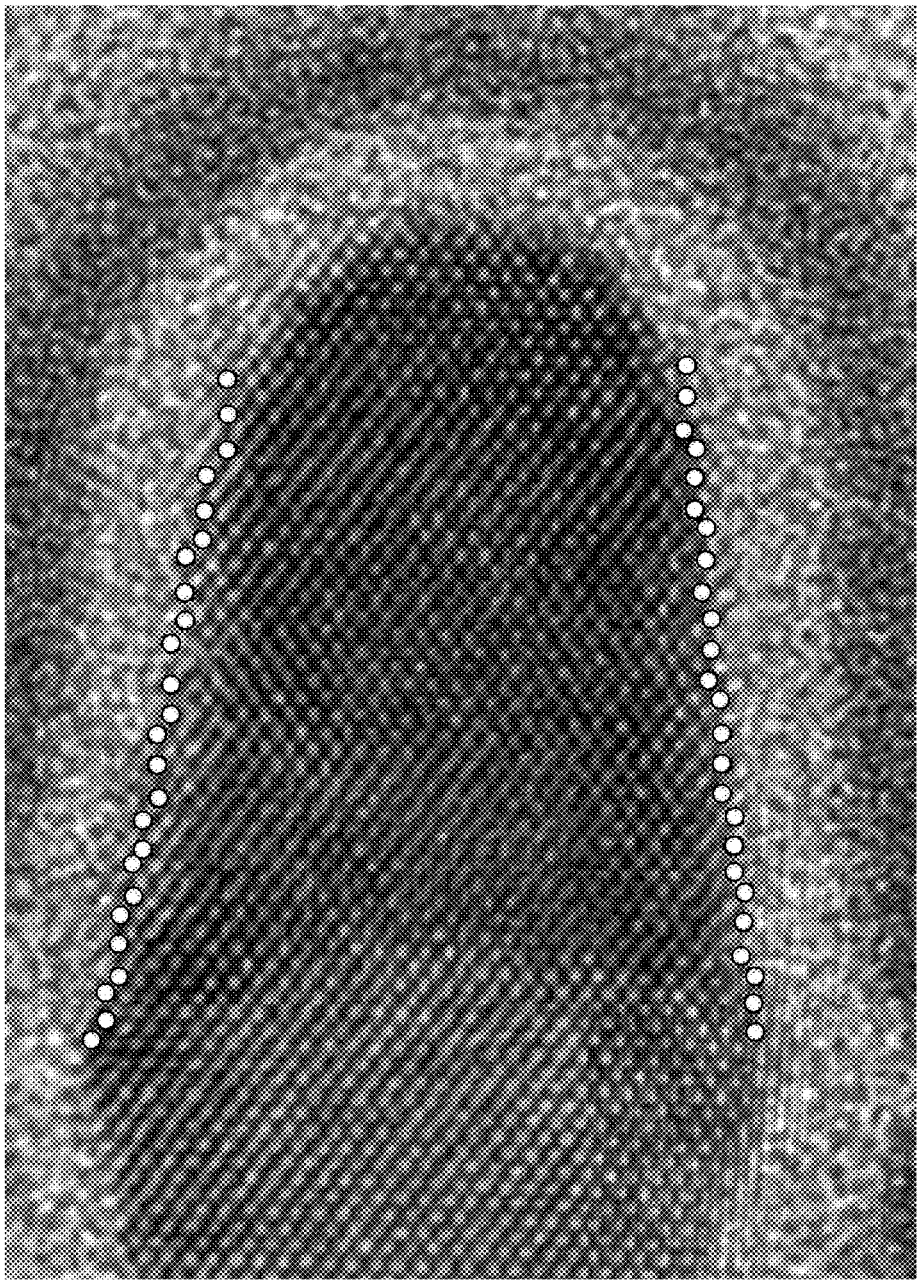


FIG. 19



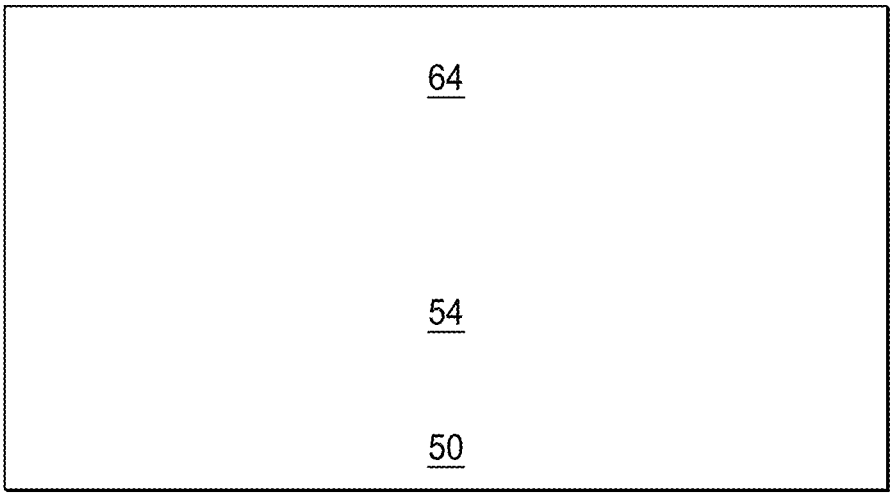


FIG. 20A

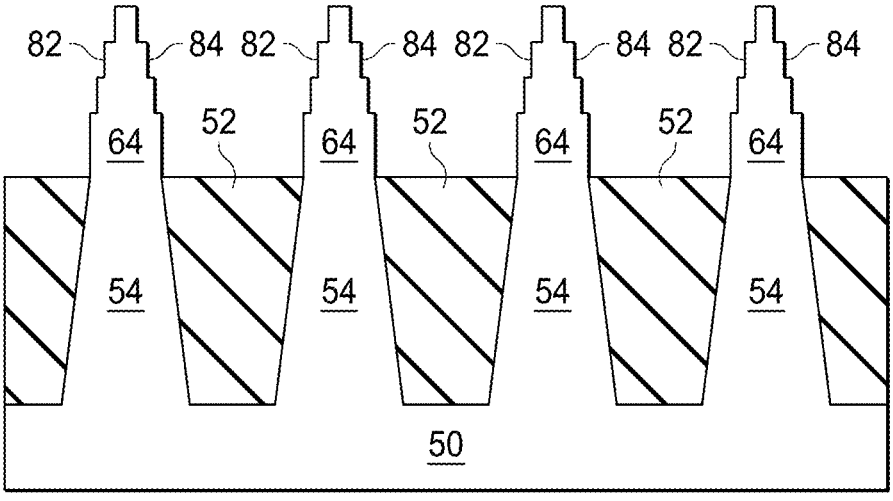


FIG. 20B

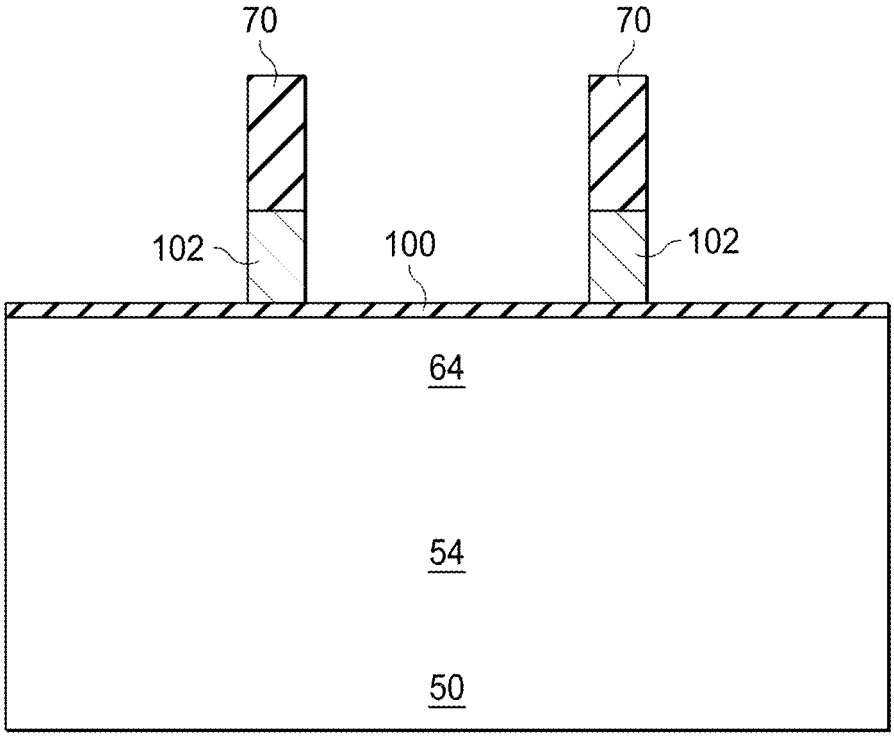


FIG. 21A

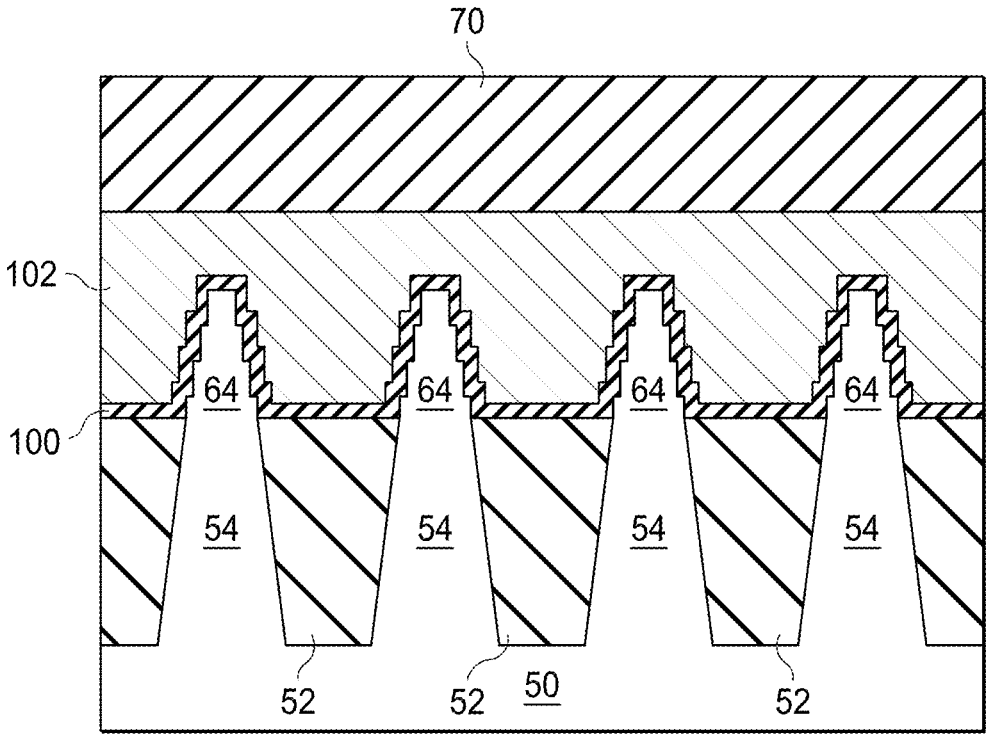


FIG. 21B

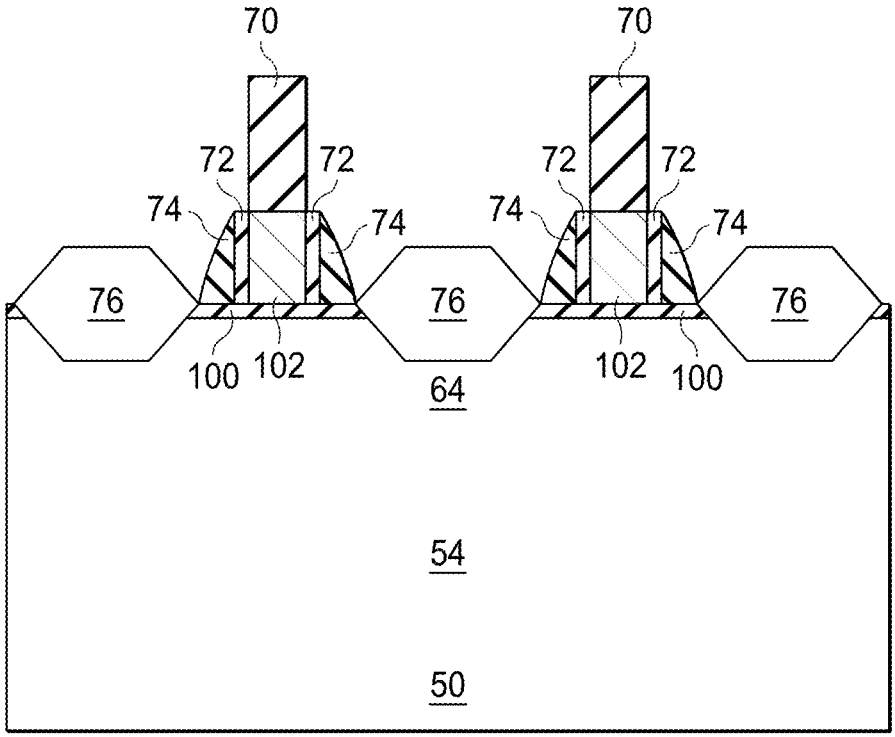


FIG. 22A

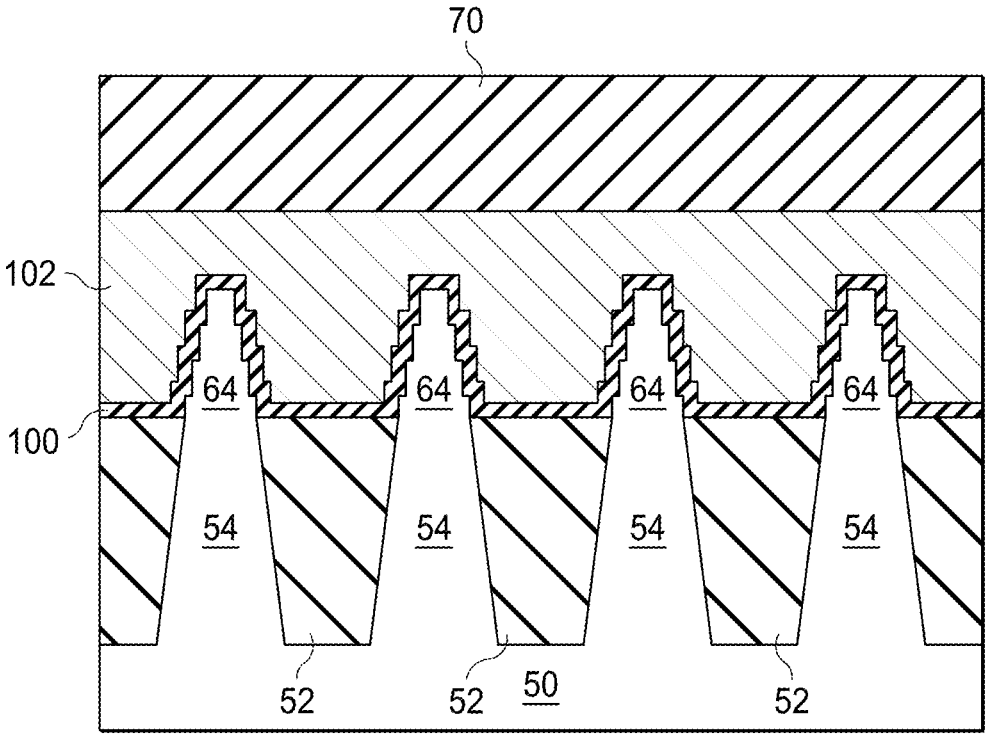


FIG. 22B

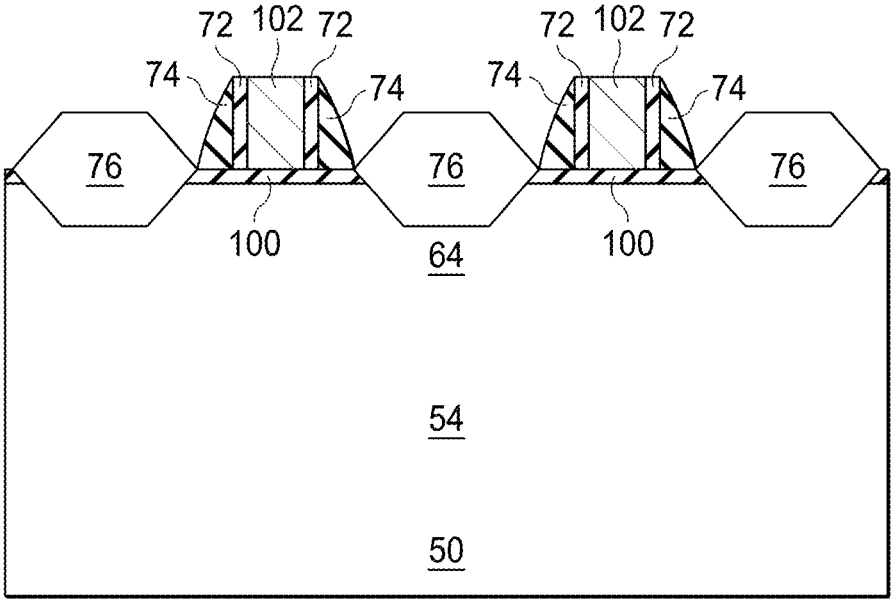


FIG. 23A

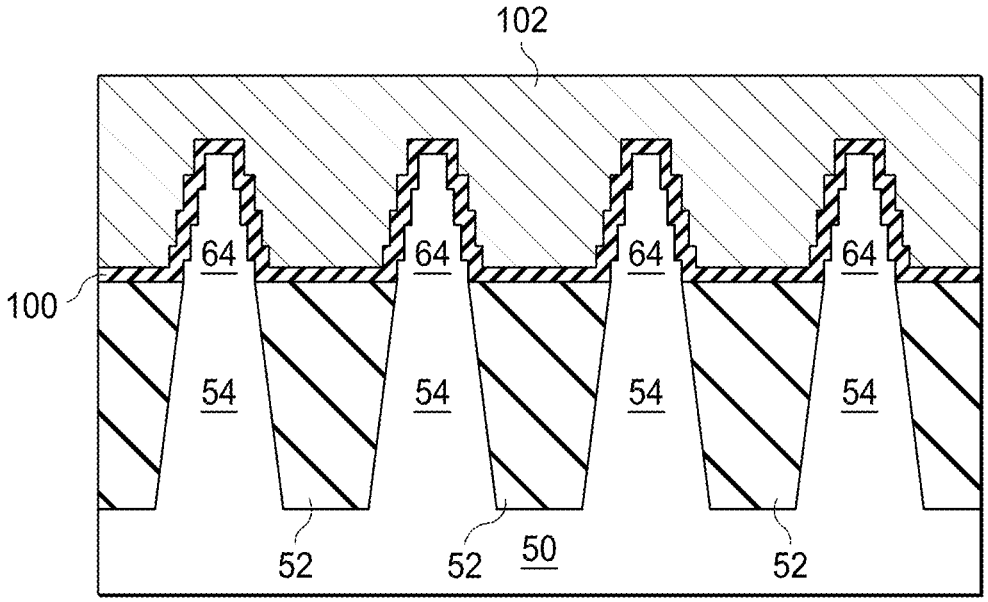


FIG. 23B

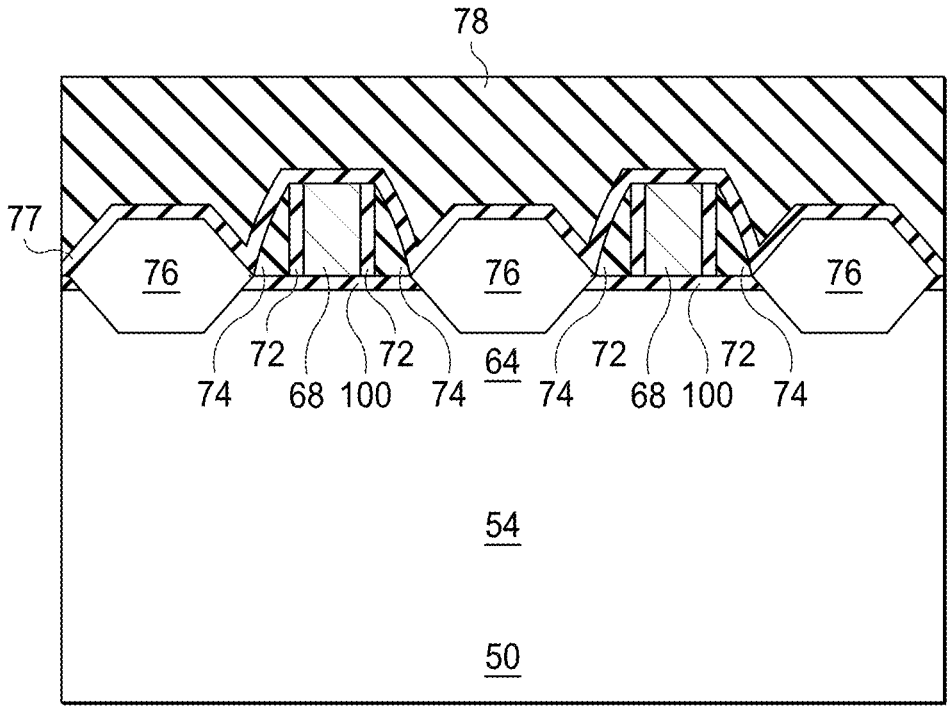


FIG. 24A

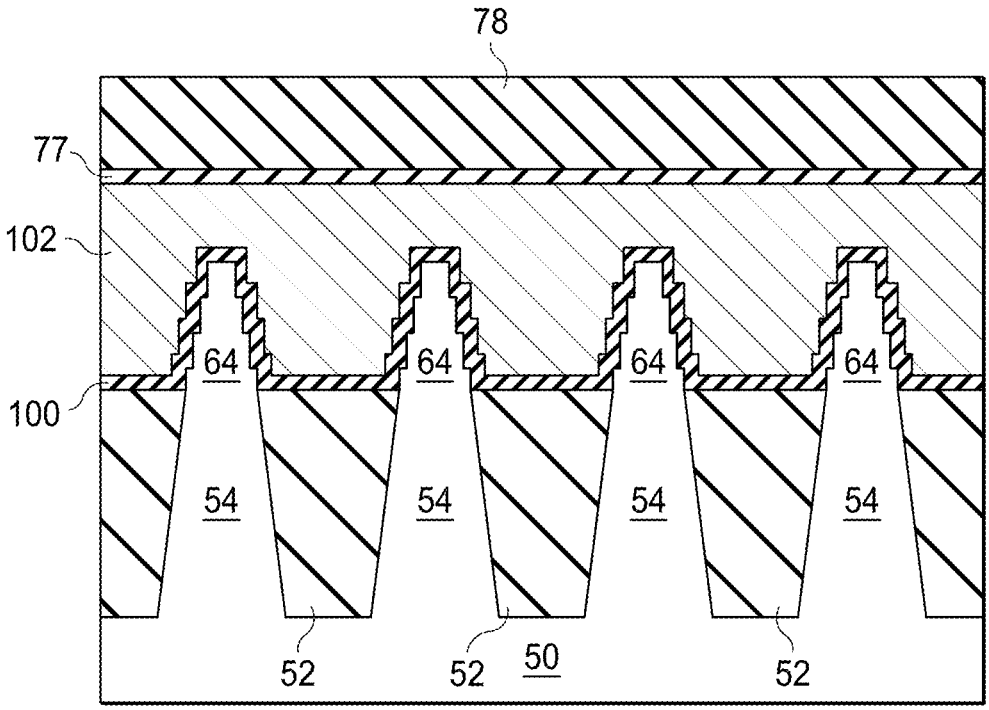


FIG. 24B

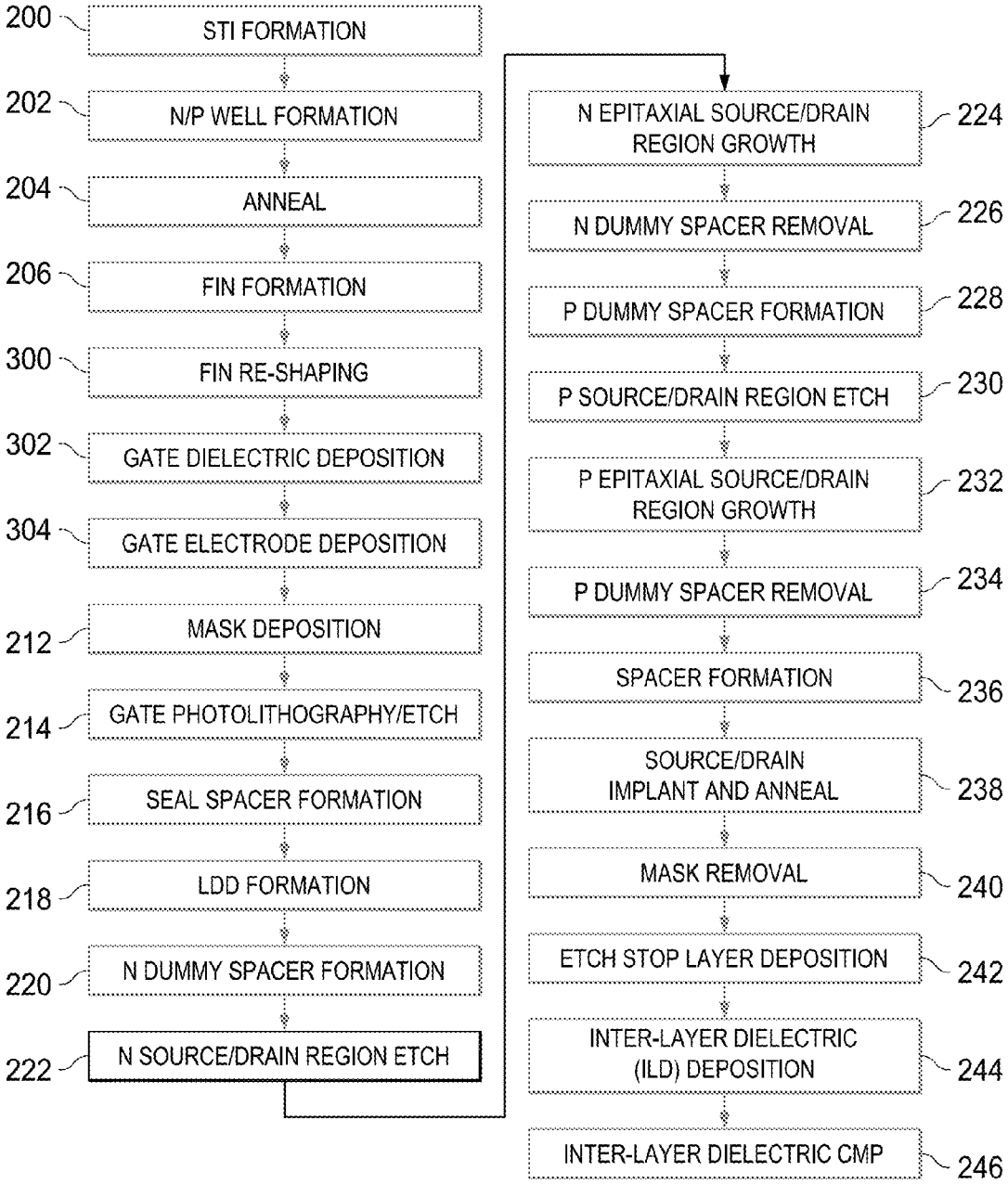

200
STI FORMATION
202
N/P WELL FORMATION
204
ANNEAL
206
FIN FORMATION
300
FIN RE-SHAPING
302
GATE DIELECTRIC DEPOSITION
304
GATE ELECTRODE DEPOSITION
212
MASK DEPOSITION
214
GATE PHOTOLITHOGRAPHY/ETCH
216
SEAL SPACER FORMATION
218
LDD FORMATION
220
N DUMMY SPACER FORMATION
222
N SOURCE/DRAIN REGION ETCH
224
N EPITAXIAL SOURCE/DRAIN REGION GROWTH
226
N DUMMY SPACER REMOVAL
228
P DUMMY SPACER FORMATION
230
P SOURCE/DRAIN REGION ETCH
232
P EPITAXIAL SOURCE/DRAIN REGION GROWTH
234
P DUMMY SPACER REMOVAL
236
SPACER FORMATION
238
SOURCE/DRAIN IMPLANT AND ANNEAL
240
MASK REMOVAL
242
ETCH STOP LAYER DEPOSITION
244
INTER-LAYER DIELECTRIC (ILD) DEPOSITION
246
INTER-LAYER DIELECTRIC CMP

FIG. 25

FINFETS AND METHODS FOR FORMING THE SAME

This application is a divisional of U.S. patent application Ser. No. 13/779,356, filed Feb. 27, 2013, entitled "FinFETs and Methods for Forming the Same," which application is hereby incorporated herein by reference in its entirety.

BACKGROUND

Semiconductor devices are used in a large number of electronic devices, such as computers, cell phones, and others. Semiconductor devices comprise integrated circuits that are formed on semiconductor wafers by depositing many types of thin films of material over the semiconductor wafers, and patterning the thin films of material to form the integrated circuits. Integrated circuits typically include field-effect transistors (FETs).

Conventionally, planar FETs have been used in integrated circuits. However, with the ever increasing density and decreasing footprint requirements of modern semiconductor processing, planar FETs may generally incur problems when reduced in size. Some of these problems include sub-threshold swing degradation, significant drain induced barrier lowering (DIBL), fluctuation of device characteristics, and leakage. Fin field-effect transistors (finFETs) have been studied to overcome some of these problems.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** is an example of a fin field-effect transistor (finFET) in a three-dimensional view;

FIGS. **2**, **3**, **4**, **5**, **6**A, **6**B, **7**A, **7**B, **8**A, **8**B, **9**A, **9**B, **10**A, **10**B, **11**A, **11**B, **12**A, **12**B, **13**A, and **13**B are cross-sectional views of intermediate stages in the manufacturing of a finFET in accordance with an exemplary embodiment;

FIG. **14** is a process flow of the process shown in FIGS. **2** through **13**B in accordance with an exemplary embodiment;

FIG. **15** is a structure of a portion of a sidewall of a fin after re-shaping according to an embodiment;

FIG. **16** is a first example of a TEM cross section of a fin that is re-shaped according to an embodiment;

FIG. **17** is a second example of a TEM cross section of a fin that is re-shaped according to an embodiment;

FIG. **18** is a third example of a TEM cross section of a fin that is re-shaped according to an embodiment;

FIG. **19** is a fourth example of a TEM cross section of a fin that is re-shaped according to an embodiment;

FIGS. **20**A, **20**B, **21**A, **21**B, **22**A, **22**B, **23**A, **23**B, **24**A, and **24**B are cross-sectional views of intermediate stages in the manufacturing of a finFET in accordance with another exemplary embodiment; and

FIG. **25** is a process flow of the process shown in FIGS. **20**A through **24**B in accordance with another exemplary embodiment.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosed subject matter, and do not limit the scope of the different embodiments.

Fin Field-Effect Transistors (finFETs) and methods of forming the same are provided in accordance with various embodiments. The intermediate stages of forming the finFETs are illustrated. Some variations of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. Although method embodiments are discussed in a particular order, various other method embodiments may be performed in any logical order and may include fewer or more steps described herein.

FIG. **1** illustrates an example of a finFET **30** in a three-dimensional view. The finFET **30** comprises a fin **34** on a substrate **32**. A gate dielectric **36** is along sidewalls and over a top surface of the fin **34**, and a gate electrode **38** is over the gate dielectric **36**. Source/drain regions **40** and **42** are disposed in opposite sides of the fin **34** with respect to the gate dielectric **36** and gate electrode **38**. FIG. **1** further illustrates reference cross-sections that are used in later figures. Cross-section A-A is along a longitudinal axis of the fin **34** and in a direction of, for example, a current flow between the source/drain regions **40** and **42**. Cross-section B-B is perpendicular to cross-section A-A and is across a channel, gate dielectric **36**, and gate electrode **38** of the finFET **30**.

FIGS. **2** through **13**B are cross-sectional views of intermediate stages in the manufacturing of a finFET in accordance with an exemplary embodiment, and FIG. **14** is a process flow of the process shown in FIGS. **2** through **13**B. FIGS. **2** through **5** illustrate cross-section B-B illustrated in FIG. **1**, except for multiple finFETs. In FIGS. **6**A through **13**B, figures ending with an "A" designation are illustrated along a similar cross-section A-A, and figures ending with a "B" designation are illustrated along a similar cross-section B-B.

FIG. **2** illustrates a substrate **50**, which may be a part of a wafer. Substrate **50** may be a semiconductor substrate, which may further be a silicon substrate, a silicon carbon substrate, a silicon germanium substrate, or a substrate formed of other semiconductor materials. The substrate **50** may be a bulk substrate, a semiconductor-on-insulator (SOI) substrate, or other acceptable substrates. The substrate **50** may be lightly doped with a p-type or an n-type impurity.

Isolation regions **52** are formed (step **200**), which extend from a top surface of substrate **50** into substrate **50**. Isolation regions **52** may be Shallow Trench Isolation (STI) regions, and are referred to as STI regions **52** hereinafter. The formation of STI regions **52** may include etching the substrate **50** to form trenches (not shown), and filling the trenches with a dielectric material to form STI regions **52**. STI regions **52** may be formed of silicon oxide deposited by a high density plasma, for example, although other dielectric materials formed according to various techniques may also be used. The portion of substrate **50** between neighboring STI regions **52** is referred to as a semiconductor strip **54** throughout the description. The top surfaces of the semiconductor strips **54** and the top surfaces of STI regions **52** may be substantially level with each other, such as by performing a chemical mechanical polish (CMP) after depositing the material of the STI regions **52**, although the surfaces may be at slightly different levels.

FIGS. **3** and **4** illustrate the formation of a P well in a first region and an N well in a second region (step **202**). Referring to FIG. **3**, a first photoresist **56** is formed over the semiconductor strips **54** and the STI regions **52** in the substrate **50**. The first photoresist **56** is patterned to expose a first region of the

substrate **50**, such as an NMOS region. The first photoresist **56** can be formed by using a spin-on technique and can be patterned using acceptable photolithography techniques. Once the first photoresist **56** is patterned, a p-type impurity implant **58** is performed in the first region, and the first photoresist **56** may act as a mask to substantially prevent p-type impurities from being implanted into a second region, such as a PMOS region. The p-type impurities may be boron, BF_2, or the like implanted in the first region to a concentration of equal to or less than 10^{18} cm^{-3}, such as between about 10^{17} cm^{-3} and about 10^{18} cm^{-3}. After the implant **58**, the first photoresist **56** may be removed, such as by an acceptable ashing process.

Referring to FIG. **4**, a second photoresist **60** is formed over the semiconductor strips **54** and the STI regions **52** in the substrate **50**. The second photoresist **60** is patterned to expose a second region of the substrate **50**, such as the PMOS region. The second photoresist **60** can be formed by using a spin-on technique and can be patterned using acceptable photolithography techniques. Once the second photoresist **60** is patterned, an n-type impurity implant **62** is performed in the second region, and the second photoresist **60** may act as a mask to substantially prevent n-type impurities from being implanted into the first region, such as the NMOS region. The n-type impurities may be phosphorus, arsenic, or the like implanted in the first region to a concentration of equal to or less than 10^{18} cm^{-3}, such as between about 10^{17} cm^{-3} and about 10^{18} cm^{-3}. After the implant **62**, the second photoresist **60** may be removed, such as by an acceptable ashing process.

After the implants in FIGS. **3** and **4**, an anneal may be performed (step **204**) to activate the p-type and n-type impurities that were implanted. The implantations may form a p-well in the NMOS region and an n-well in the PMOS region.

In FIG. **5**, the STI regions **52** are recessed such that respective fins **64** protrude from between neighboring STI regions **52** to form the fins **64** (step **206**). The STI regions **52** may be recessed using an acceptable etching process, such as one that is selective to the material of the STI regions **52**. For example, a chemical oxide removal using a Tokyo Electron CERTAS or an Applied Materials SICONI tool or dilute hydrofluoric acid may be used.

A person having ordinary skill in the art will readily understand that the process described with respect to FIGS. **2** through **5** is just one example of how fins **64** may be formed. In other embodiments, a dielectric layer can be formed over a top surface of the substrate **50**; trenches can be etched through the dielectric layer; homoepitaxial structures can be epitaxially grown in the trenches; and the dielectric layer can be recessed such that the homoepitaxial structures protrude from the dielectric layer to form fins. In still other embodiments, heteroepitaxial structures can be used for the fins. For example, the semiconductor strips **54** in FIG. **2** can be recessed, and a material different from the semiconductor strips **54** may be epitaxially grown in their place. In an even further embodiment, a dielectric layer can be formed over a top surface of the substrate **50**; trenches can be etched through the dielectric layer; heteroepitaxial structures can be epitaxially grown in the trenches using a material different from the substrate **50**; and the dielectric layer can be recessed such that the heteroepitaxial structures protrude from the dielectric layer to form fins. In some embodiments where homoepitaxial or heteroepitaxial structures are epitaxially grown, the grown materials may be in situ doped during growth, which may obviate the implantations discussed in FIGS. **3** and **4** although in situ and implantation doping may be used together. Still further, it may be advantageous to epitaxially grow a material in the NMOS region different from the material in the PMOS region. In various embodiments, the fins **64** may comprise silicon germanium (Si_xGe_{1-x}, where x can be between approximately 0 and 100), silicon carbide, pure or substantially pure germanium, a III-V compound semiconductor, a II-VI compound semiconductor, or the like. For example, the available materials for forming III-V compound semiconductor include, but are not limited to, InAs, AlAs, GaAs, InP, GaN, InGaAs, InAlAs, GaSb, AlSb, AlP, GaP, and the like.

Referring to FIGS. **6**A and **6**B, a dummy gate dielectric layer **66** is formed (step **208**) on the fins **64**. The dummy gate dielectric layer **66** may be, for example, silicon oxide, silicon nitride, a combination thereof, or the like, and may be deposited or thermally grown according to acceptable techniques. Dummy gates **68** are formed over the dummy gate dielectric layer **66**, and masks **70** are formed over the dummy gates **68**. A material of the dummy gates **68** may be deposited (step **210**) over the dummy gate dielectric layer **66** and then planarized, such as by a CMP. A material of the masks **70** may be deposited (step **212**) over the layer of the dummy gates **68**. The material of the masks **70** then may be patterned using acceptable photolithography and etching techniques. The pattern of the masks **70** then may be transferred to the material of the dummy gates **68** by an acceptable etching technique. These photolithography and etching techniques may form the dummy gates **68** and masks **70** (step **214**). Dummy gates **68** may be formed of, for example, polysilicon, although other materials that have a high etching selectivity from the etching of STI regions **52** may also be used. The masks **70** may be formed of, for example, silicon nitride or the like. The dummy gates **68** cover respective channel regions of the fin **64**. The dummy gates **68** may also have a lengthwise direction substantially perpendicular to the lengthwise direction of respective fins **64**.

Referring to FIGS. **7**A and **7**B, gate seal spacers **72** can be formed (step **216**) on exposed surfaces of respective dummy gates **68**. A thermal oxidation or a deposition followed by an anisotropic etch may form the gate seal spacers **72**. Implants for lightly doped source/drain (LDD) regions may be performed (step **218**). Similar to FIGS. **3** and **4**, a mask may be formed over the PMOS region while exposing the NMOS region, and n-type impurities may be implanted into the exposed fins **64**. The mask may then be removed. Subsequently, a mask may be formed over the NMOS region while exposing the PMOS region, and p-type impurities may be implanted into the exposed fins **64**. The mask may then be removed. The n-type impurities may be the any of the n-type impurities previously discussed, and the p-type impurities may be the any of the p-type impurities previously discussed. The lightly doped source/drain regions may have a concentration of impurities of from about 10^{15} cm^{-3} to about 10^{16} cm^{-3}. An anneal may activate the implanted impurities.

Epitaxial source/drain regions **76** are formed in the fins **64**, wherein each dummy gate **68** is disposed between respective neighboring pairs of the epitaxial source/drain regions **76**. Epitaxial source/drain regions **76** in the NMOS region may be formed by masking the PMOS region and conformally depositing a dummy spacer layer in the NMOS region followed by an anisotropic etch to form dummy gate spacers (step **220**) (not shown in FIGS. **7**A and **7**B) along sidewalls of the dummy gates **68** in the NMOS region. Then, source/drain regions of the fins **64** in the NMOS region are etched (step **222**) to form recesses. The epitaxial source/drain regions **76** in the NMOS region are epitaxially grown (step **224**) in the recesses. The epitaxial source/drain regions **76** may comprise any material appropriate for n-type finFETs. For example, if

the fin is silicon, the epitaxial source/drain regions **76** may comprise silicon, SiC, SiCP, or the like. The epitaxial source/drain regions **76** may have surfaces raised from respective surfaces of the fins **64** and may have facets. Subsequently, the dummy gate spacers in the NMOS region are removed (step **226**), for example, by an etch, as is the mask on the PMOS region.

Epitaxial source/drain regions **76** in the PMOS region may be formed by masking the NMOS region and conformally depositing a dummy spacer layer in the PMOS region followed by an anisotropic etch to form dummy gate spacers (step **228**) (not shown in FIGS. **7**A and **7**B) along sidewalls of the dummy gates **68** in the PMOS region. Then, source/drain regions of the fins **64** in the PMOS region are etched (step **230**) to form recesses. The epitaxial source/drain regions **76** in the PMOS region are epitaxially grown (step **232**) in the recesses. The epitaxial source/drain regions **76** may comprise any material appropriate for p-type finFETs. For example, if the fin is silicon, the epitaxial source/drain regions **76** may comprise $SiGe_x$, $SiGe_xB$, or the like. The epitaxial source/drain regions **76** may have surfaces raised from respective surfaces of the fins **64** and may have facets. Subsequently, the dummy gate spacers in the PMOS region are removed (step **234**), for example, by an etch, as is the mask on the NMOS region.

Gate spacers **74** are formed (step **236**) on the gate seal spacers **72** along sidewalls of the dummy gates **68**. The gate spacers **74** may be formed by conformally depositing a material and subsequently anisotropically etching the material. The material of the gate spacers **74** may be silicon nitride, SiCN, a combination thereof, or the like.

The epitaxial source/drain regions **76** and/or fins **64** may be implanted with dopants to form source/drain regions, similar to the process previously discussed for forming lightly doped source/drain regions, followed by an anneal (step **238**). The source/drain regions may have an impurity concentration of between about 10^{19} cm^{-3} and about 10^{21} cm^{-3}. The n-type impurities for source/drain regions in the NMOS region may be any of the n-type impurities previously discussed, and the p-type impurities for source/drain regions in the PMOS region may be any of the p-type impurities previously discussed. In other embodiments, the epitaxial source/drain regions **76** may be in situ doped during growth.

In FIGS. **8**A and **8**B, the masks **70** are removed (step **240**), for example, by an etch selective to the material of the masks **70**.

FIGS. **9**A and **9**B illustrate an etch stop layer **77** is conformally or non-conformally deposited (step **242**) over the structure illustrated in FIGS. **8**A and **8**B, and an Inter-Layer Dielectric (ILD) **78** is deposited (step **244**) over the etch stop layer **77**. The etch stop layer **77** may be silicon nitride, SiOn, SiCN, a combination thereof, and the like. ILD **78** is formed of a dielectric material such as Phospho-Silicate Glass (PSG), Boro-Silicate Glass (BSG), Boron-Doped Phospho-Silicate Glass (BPSG), undoped Silicate Glass (USG), or the like.

Referring to FIGS. **10**A and **10**B, a CMP may be performed (step **246**) to level the top surface of ILD **78** with the top surfaces of the dummy gates **68**. The CMP may also remove portions of the etch stop layer **77** that are directly above the dummy gates **68**. Accordingly, top surfaces of the dummy gates **68** are exposed through the ILD **78** and the etch stop layer **77**.

Next, referring to FIGS. **11**A and **11**B, the dummy gates **68**, gate seal spacers **72**, and portions of the dummy gate dielectric **66** directly underlying the dummy gates **68** are removed in an etching step(s), so that recesses **80** are formed. Each recess **80** exposes a channel region of a respective fin **64**. Each channel region is disposed between neighboring pairs of epitaxial source/drain regions **76**. During the removal, the dummy gate dielectric **66** may be used as an etch stop layer when the dummy gates **68** are etched (step **248**). The dummy gate dielectric **66** and gate seal spacers **72** may then be removed (step **250**) after the removal of the dummy gates **68**.

In FIGS. **12**A and **12**B, the channel regions of the fins **64** are re-shaped (step **252**). Each channel region of the fins **64** is re-shaped to have a cross-section that intersects a longitudinal axis of the fin **64** (e.g., in a direction of current flow between the source/drain regions during operation of the finFET) that is substantially trapezoidal or triangular in shape. For example, the channel region of the fin **64** may comprise substantially a trapezoidal prism or a triangular prism. Sidewalls **82** and **84** may be respective rectangular faces of a prism, and a base of the prism may be a rectangular area disposed in the fin **64** connecting the sidewalls **82** and **84**. FIG. **12**B shows a stair-step illustration of the sidewalls **82** and **84**. Some embodiments may have substantially smooth sidewalls **82** and **84**, and other embodiments may have sidewalls **82** and **84** with more pronounced stair-step increments. Other aspects of the structure of a re-shaped fin will be discussed in more detail with respect to FIGS. **15** through **19** below.

The fin re-shaping may be performed using one or more of a wet etch, a dry etch, or an anneal. A wet etch may comprise an immersion in a solution comprising an etching species. The etching species can comprise ammonium hydroxide (NH_4OH), an ammonia peroxide mixture (APM), hydrochloric acid (HCl), dilute hydrofluoric acid (dHF), a combination thereof, or the like. The etching species can have a concentration between about 0.2 percent and about 20 percent in the solution. The wet etch can include immersion in the solution from about 20 seconds to about 600 seconds and can be at a temperature of about 20° C. to about 60° C. A dry etch may comprise a plasma process, such as inductively coupled plasma (ICP), transformer coupled plasma (TCP), electron cyclotron resonance (ECR), reactive ion etch (RIE), the like, or a combination thereof. The plasma process may use reaction gases including boron trichloride (BCl_3), chloride (Cl_2), hydrogen bromide (HBr), oxygen (O_2), the like, or a combination thereof. The plasma process may use a pressure between about 3 mTorr and about 100 mTorr, use a power of about 300 W to about 1500 W, and may use a frequency of about 2 kHz to about 13.6 MHz. An anneal may comprise heating at a temperature greater than or equal to 500° C. for about a few milliseconds, such as for a high temperature anneal at temperatures between about 800° C. and about 1200° C., to about 12 hours, such as for a lower temperature anneal at temperatures between about 500° C. and about 800° C.

FIGS. **13**A and **13**B illustrate the formation of gate dielectric layer **86** and gate electrodes **88**. Gate dielectric layer **86** is deposited (step **254**) conformally in recesses **80**, such as on the top surfaces and the sidewalls of fins **64** and on sidewalls of the gate spacers **74**, and on a top surface of the ILD **78**. In accordance with some embodiments, gate dielectric layer **86** comprises silicon oxide, silicon nitride, or multilayers thereof. In other embodiments, gate dielectric layer **86** comprises a high-k dielectric material, and in these embodiments, gate dielectric layer **86** may have a k value greater than about 7.0, and may include a metal oxide or a silicate of Hf, Al, Zr, La, Mg, Ba, Ti, Pb, and combinations thereof. The formation methods of gate dielectric layer **86** may include Molecular-Beam Deposition (MBD), Atomic Layer Deposition (ALD), Plasma Enhanced Chemical Vapor Deposition (PECVD), and the like. Next, gate electrodes **88** are deposited (step **256**) over

gate dielectric layer **86**, and fills the remaining portions of the recesses **80**. Gate electrodes **88** may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof, or multi-layers thereof. After the filling of gate electrodes **88**, a CMP may be performed to remove the excess portions of gate dielectric layer **86** and the material of gate electrodes **88**, which excess portions are over the top surface of ILD **78**. The resulting remaining portions of material of gate electrodes **88** and gate dielectric layer **86** thus form replacement gates of the resulting finFETs.

Although not explicitly shown, a person having ordinary skill in the art will readily understand that further processing steps may be performed on the structure in FIGS. **13**A and **13**B. For example, an etch stop layer may be formed over and adjoining the gates and ILD. Inter-Metal Dielectrics (IMD) and their corresponding metallizations may be formed over the etch stop layer.

FIG. **15** illustrates a structure of a major surface portion of a sidewall **84** of a fin **64** after re-shaping. The structure shows the crystalline structure (e.g., dots being atoms and dashed lines being the lattice) of the fin **64**, which may include, for example, silicon or germanium. In an embodiment, the major surface portion of the sidewall **84** of the fin **64** is a portion of the sidewall **64** between the substrate **50** and a corner, e.g. a rounded corner, at a top surface of the fin. For ease of reference, FIG. **15** includes axes X, Y, and Z. The substrate **50** is in the negative Y direction from this structure, and a top surface of the substrate **50**, e.g., which may include top surfaces of STI regions **52**, is in an X-Z plane.

The structure includes shift locations **90** inward toward a center of the fin **64** (e.g., in the positive X direction) along the sidewall. These shift locations **90** are places along the sidewall **84** where the exterior sidewall surface shifts inward one lattice constant. For example, shift location **90** may shift the exterior sidewall surface from a first Y-Z plane **91** to a second Y-Z plane **92**, from the second Y-Z plane **92** to a third Y-Z plane **93**, from the third Y-Z plane **93** to a fourth Y-Z plane **94**, etc. In other embodiments, the shift may be outward from the fin **64** instead of inward. Further, the sidewall **84** may comprise any combination of inward shifts and outward shifts. The amount of the shifts **90** in the +/−X direction may be at least one lattice constant to several lattice constants, for example, the distance between neighboring pairs of the Y-Z planes **91** through **94** may be at least one lattice constant to several lattice constants. The amount of the shifts **90** in the +/−X direction may be constant between the shifts **90** or may vary between shifts **90**. The distance between neighboring shifts **90** in the +/−Y direction may be any distance, such as between 2 atoms and 20 atoms in the lattice. The distances between neighboring shifts **90** in the +/−Y direction may be constant throughout the sidewall **84**, e.g., may have a repeating period, or may vary.

FIG. **16** is a first example of a TEM cross section of a fin that is re-shaped according to an embodiment. Distinct, white markers have been added to the image to delineate atoms in the crystalline structure along the sidewalls of the fins. In this embodiment, each sidewall comprises inward shifts and outward shifts. Further, the distances between shifts vary.

FIG. **17** is a second example of a TEM cross section of a fin that is re-shaped according to an embodiment. As with FIG. **16**, distinct, white markers have been added to the image to delineate atoms in the crystalline structure along the sidewalls of the fins. In this embodiment, each sidewall comprises only inward shifts. Further, the distances between shifts vary, although segments of the sidewalls have a repeating distance between shifts (e.g., 4 atoms).

FIGS. **18** and **19** are a third and fourth example, respectively, of TEM cross sections of fins that are re-shaped according to embodiments. As with above, distinct, white markers have been added to the images to delineate atoms in the crystalline structure along the sidewalls of the fins. These examples show other configurations of sidewalls that are contemplated within the scope of various embodiments.

FIGS. **20**A through **24**B are cross-sectional views of intermediate stages in the manufacturing of a finFET in accordance with another exemplary embodiment, and FIG. **25** is a process flow of the process shown in FIGS. **20**A through **24**B. In FIGS. **20**A through **24**B, figures ending with an "A" designation are illustrated along a similar cross-section A-A as shown in FIG. **1**, and figures ending with a "B" designation are illustrated along a similar cross-section B-B as shown in FIG. **1**. The process proceeds through FIGS. **2** through **5** (steps **200** through **206**) as previously discussed.

In FIGS. **20**A and **20**B, the fins **64** are re-shaped (step **300**), as in FIGS. **12**A and **12**B. However, in this embodiment, because the whole of each fin **64** is exposed to the re-shaping process, the entire fin **64** may be re-shaped.

In FIGS. **21**A and **21**B, a gate dielectric layer **100** is deposited (step **302**) on the fins **64**. The gate dielectric layer **100** may be, for example, any of the materials and formed as previously discussed for gate dielectric layer **86** with respect to FIGS. **13**A and **13**B. A material of gate electrodes **102** is deposited (step **304**) over the gate dielectric layer **100**, and a material of masks **70** is deposited (step **212**) over the material of gate electrodes **102**. A material of the gate electrodes **102** may be deposited over the gate dielectric layer **100** and then planarized, such as by a CMP. A material of the masks **70** may be deposited over the layer of the gate electrodes **102**. The material of the masks **70** then may be patterned using acceptable photolithography and etching techniques. The pattern of the masks **70** then may be transferred to the material of the gate electrodes **102** by an acceptable etching technique. These photolithography and etching techniques may form the gate electrodes **102** and masks **70** (step **214**). Gate electrodes **102** may be formed of, for example, polysilicon, any material previously discussed with respect to gate electrodes **88** in FIGS. **13**A and **13**B, or the like. The gate electrodes **102** cover respective channel regions of the fin **64**. The gate electrodes **102** may also have a lengthwise direction substantially perpendicular to the lengthwise direction of respective fins **64**.

With reference to FIGS. **22**A and **22**B, the components therein identified are the same as or similar to similarly numbered components in FIGS. **7**A and **7**B, and the components in FIGS. **22**A and **22**B may be formed in the same or similar manner (steps **216** through **238**) as discussed with respect to FIGS. **7**A and **7**B. Any necessary modification would be readily understood by a person having ordinary skill in the art, and thus, explicit discussion here is omitted for brevity.

In FIGS. **23**A and **23**B, the mask **70** is removed (step **240**), similar to what was discussed in FIGS. **8**A and **8**B.

In FIGS. **24**A and **24**B, an etch stop layer **77** and ILD **78** are formed (steps **242** and **244**) similar to what is discussed in FIGS. **9**A and **9**B. After the ILD **78** is deposited, the ILD **78** may undergo a CMP (step **246**), and a portion of the ILD **78** may remain directly over the gate electrodes **102**.

Various embodiments that have a re-shaped fin in a finFET may have increased electrical characteristics and performance compared to a conventional finFET. For example, it is believed that increased surface roughness can increase mobility. An increased surface roughness may increase phonon scattering, thereby increasing the mobility. Hence, in some

embodiments where the fin has been re-shaped as discussed above, the finFET can have increased electrical characteristics and performance.

According to an embodiment, a structure comprises a substrate, a fin, a gate dielectric, and a gate electrode. The substrate comprises the fin. The fin has a major surface portion of a sidewall, and the major surface portion comprises at least one lattice shift. The at least one lattice shift comprises an inward or outward shift relative to a center of the fin. The gate dielectric is on the major surface portion of the sidewall. The gate electrode is on the gate dielectric.

According to another embodiment, a structure comprises a fin on a substrate, a gate dielectric on a major surface portion of a sidewall of the fin, and a gate electrode on the gate dielectric. The major surface portion comprises atoms in multiple parallel planes. The multiple parallel planes are perpendicular to a major surface of the substrate, and neighboring pairs of the multiple parallel planes are separated by at least one lattice constant. A first group of the atoms are in a first one of the multiple parallel planes, and a second group of the atoms are in a second one of the multiple parallel planes.

According to a further embodiment, a method comprises forming a fin on a substrate; after forming the fin, re-shaping the fin to have a major surface portion of a sidewall; forming a dielectric on the major surface portion of the sidewall; and forming a gate electrode on the dielectric. The major surface portion of the sidewall has a plurality of lattice shift locations. Each of the plurality of lattice shift locations comprises an inward or outward lattice shift relative to a center of the fin.

Although the present embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method comprising:
- forming a fin on a substrate;
- after forming the fin, re-shaping the fin to have a surface portion of each sidewall of the fin with a plurality of lattice shift locations, the surface portion of each sidewall extending from the to of each sidewall, each of the plurality of lattice shift locations comprising an inward or outward shift relative to a center of the fin;
- forming a dielectric on the surface portion of the sidewall; and
- forming a gate electrode on the dielectric.

2. The method of claim **1**, wherein the re-shaping the fin comprises a wet etch.

3. The method of claim **1**, wherein the re-shaping the fin comprises a dry etch.

4. The method of claim **1**, wherein the re-shaping the fin comprises an anneal.

5. The method of claim **1**, wherein the re-shaping the fin increases a surface roughness of the fin.

6. The method of claim **1** further comprising:
- forming a dummy dielectric on the fin;
- forming a dummy gate on the dummy dielectric; and
- removing the dummy gate and the dummy dielectric, the re-shaping the fin being performed after removing the dummy gate and the dummy dielectric.

7. The method of claim **1**, wherein the plurality of lattice shift locations comprises a plurality of inward lattice shifts relative to the center of the fin when traversing the plurality of lattice shifts in a direction away from the substrate.

8. The method of claim **1**, wherein the plurality of lattice shift locations comprises a plurality of outward lattice shifts relative to the center of the fin when traversing the plurality of lattice shifts in a direction away from the substrate.

9. The method of claim **1**, wherein the plurality of lattice shift locations comprises a combination of inward lattice shifts and outward lattice shifts relative to the center of the fin.

10. A method comprising:
- forming a fin on a substrate, the fin having a first exterior side surface in a channel region of the fin;
- increasing a surface roughness of the fin in the channel region by re-shaping the entire surface of the channel region of the fin to have a second exterior side surface with a plurality of lattice shifts;
- forming a gate dielectric on the second exterior side surface in the channel region; and
- forming a gate electrode on the gate dielectric.

11. The method of claim **10**, wherein the increasing the surface roughness of the fin comprises using a wet etch.

12. The method of claim **10**, wherein the increasing the surface roughness of the fin comprises using a dry etch.

13. The method of claim **10**, wherein the increasing the surface roughness of the fin comprises using an anneal.

14. The method of claim **10** further comprising:
- forming a dummy dielectric on the first exterior side surface in the channel region;
- forming a dummy gate on the dummy dielectric; and
- removing the dummy gate and the dummy dielectric, the increasing the surface roughness of the fin being performed after the removing.

15. The method of claim **10**, wherein the second exterior side surface further extends to a region of the fin outside of the channel region.

16. A method comprising:
- forming a fin in a substrate, the fin being proximate an isolation region, the fin having a first exterior surface protruding above the isolation region;
- forming a dummy dielectric on the first exterior surface of the fin;
- forming a dummy gate on the dummy dielectric;
- removing the dummy gate and the dummy dielectric;
- after the removing, causing the fin to have a second exterior surface protruding above the isolation region, the second exterior surface deviating from the first exterior surface by a plurality of lattice shifts and comprising a portion of a top surface of the fin and a portion of a sidewall of the fin;
- forming a gate dielectric on the second exterior surface; and
- forming a gate electrode on the gate dielectric.

17. The method of claim **16**, wherein the causing the fin to have the second exterior surface comprises a wet etch, a dry etch, an anneal, or a combination thereof.

18. The method of claim **16**, wherein the second exterior surface has a greater surface roughness than the first exterior surface.

19. The method of claim **16**, wherein the plurality of lattice shifts comprises a first lattice shift and a second lattice shift, the second lattice shift being distally located from the isolation region relative to the first lattice shift, the first lattice shift being an inward lattice shift relative to a center line of the fin when traversing the plurality of lattice shifts in a direction from the first lattice shift to the second lattice shift, the second lattice shift being an outward lattice shift relative to the center line of the fin when traversing the plurality of lattice shifts in the direction.

20. The method of claim **16**, wherein each of the plurality of lattice shifts is an inward lattice shift relative to a center line of the fin when traversing the plurality of lattice shifts in a direction from proximate the isolation region to distally from the isolation region.

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